University of Southern California
Viterbi School of Engineering
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EE505 – Analog, Mixed Signal, and RF Integrated Circuit Tapeout
Course Syllabus
Summer 2025

Abstract

EE505 is an introductory tapeout class. Complete systematic tape-out flow including schematic design, simulation, layout and post-layout verification of analog, mixed-signal or radio-frequency (RF) integrated circuits (IC) is covered. However, the course is mainly taught with an emphasis in analog design, combined with digital and RF. The goal in EE505 is to participate in an actual tapeout of your work by submitting for fabrication so that it may be tested in the future. We plan to use the TSMC 180nm and 65nm CMOS process design kit (PDK) along with Cadence Design Tools at USC.

Course Administration

EE505 is a 2 hour "studio" format on Tuesdays and Thursdays, in which lecture is taught by the instructor for the first half of the class and remaining time is held as an in-class workshop with student project updates where help with the chip layout is received—all in the same setting. All classes meet in OHE230 from 12:00-2:05pm. The class will be recorded on Zoom via Brightspace so students can review the lecture and participate remotely as needed. The prerequisite is EE536a. **In some special cases, a prerequisite of EE477L with an undergraduate analog circuit design course, such as EE348L, may work—in this case, please contact the course instructor at schober@usc.edu and speak to your course advisor for possible D-clearance.**

The EE505 grade is based on the following components:

Project 1 (Due: June 5, 2025): "Differential" aka "Balanced" Transimpedance Amplifier (TIA): 20%

Project 2 (Due: June 19, 2025): Complimentary Charge Injection Voltage Amplifier (C^2iAmp): 20%

Project 3 (Due: July 10, 2025): Fully Differential Operational Amplifier with Digital Clocking and Switched Capacitors (OpAmp): 20%

Project 4 (Due: July 31, 2025): Ring Voltage Controlled Oscillator (VCO) w/Resistor, Capacitor, and/or Inductor Cross-Coupling: 20%

End of the Semester Project Team Presentation/Design Review on Zoom (Due: August 5, 2025 – In person or pre-recorded for the class is fine and presented) and Writeup (Due: August 7, 2025 – No lecture/lab this day, just submission of the final writeup of all your/your team's work): 20%

For each of the 4 Projects, there will be a "soft" deadline (dates shown above) with the completion of the given circuit blocks and sizing assigned to you in class as needed. Each of the projects will go through 1-2 design reviews depending on the complexity of the circuits—dates will be announced in class for this. Participating in the design reviews are part of the grades for each of your projects. When the projects are due students can upload your design rule check (DRC) and layout versus schematic (LVS) clean initial Graphic Design System (gds), schematics, and any post-layout simulation zipped files to the course Brightspace website where the TA will create a submission folder for each project to be reviewed by the professor. The sites will remain open all semester to update your circuit layout designs and files if you desire up until the final day of class when all projects are due after the soft deadlines. The final design portion of the grades for each project will be done at this final hard submission ("hard" deadline is August 7, 2025).

The first, second, and fourth projects will be an individual assignments. The third (OpAmp) project will be a team-based project where circuit blocks are assigned to smaller groups of 2-4 students to complete the overall top-level project. For all of the IC layout projects will be explained further in detail in class, in that the circuit design and basic sizing will be given to you and your work as an individual (or team) is to replicate the schematic in Cadence and build the physical design (i.e. layout) of the given blocks which will be placed in an IC for fabrication once all rule checks have been verified as clean. Each project deadline will also require a brief report writeup detailing your layout design.

As we move through the semester, we will be working on placing one or more designs out of our projects onto a top level chip layout. This summer our focus will be on making various sizes of the C^2iAmps and possibly the OpAmp in preparation for tapeout. To do this we will be finalizing our designs and placing pads and conducting the necessary antenna/electric rule checks (ERC) in addition to the DRC/LVS checks above. This will be a whole class effort and may actually continue on up until the tapeout after the class finishes to prepare the final submission. After the end of the course, it is on a volunteer basis if you would like to particiate in getting the chip gds tapeout on the chosen fab date. The instructor will give more detail regarding this in-class. If a student wants to put any other design on the chip, please speak to the instructor as at times there is space to do so. In those cases, the design must be shown in detail to the instructor and it must be clean and the student must participate in the tapeout in the Fall.

For success in this class, it is expected that you know how ahead of time to characterize and simulate basic analog circuits in Cadence via EE536a, as these can supplement your project deadline submittals for post-layout verification. In some cases, EE477L with a undergrad class in EE348L or similar can work (again—see the instructor if this is you).

If you are a distance student or are a PhD student travelling for a conference, you can log on to Zoom to watch/participate during the class time (and at other times if needed) along with teaming with an in-class student so that you can work together to stay up-to-date. It is your responsibility to make sure you stay in contact with your teammate and the professor in getting your projects completed if you choose to do this and work remotely. Please notify the instructor if this is you.

The TA and instructor will help monitor a Brightspace EE505 discussion board where you can post any questions you have regarding the projects, so that everyone, including all students can help answer any issues that may arise with Cadence and the pdk as we go together through the semester. The goal is to

work as a team in this respect with the whole class much like a group in a fabless semiconductor company to successfully reach a tapeout in the short 10 weeks we are given for the summer session. To meet this goal, this requires helping each other. The actual tapeout is dependent on the fab and who we use to tapeout with such as MUSE and TSMC and the technology node, and this generally happens over the course of the Fall semester so that the chips are returned in time for testing in EE599 (see below). Nevertheless, we ask that you first post in the discussion board to ask any questions or share information you may encounter that can help others here instead of emailing directly the TA and Professor if it has to do with work on the assigned projects.

In some cases, doctoral students may use work they are doing in their research groups to complete the assignments. If this is you, please speak to the instructor and we will work out an alternative layout design schedule for you and designs that you can tapeout with the class.

Apart from numerical grades for the assignments above, final class letter grades will be posted on Brightspace by August 13, 2025. It is the student's responsibility to verify (and possibly contest) these grades **before** the grade deadline on August 15, 2025. **Once assigned, a letter grade will not be changed except for grossly erroneous circumstances.**

The last day to drop the class without a W grade is June, 27, 2025, without a refund (June 6, 2025, with a refund). The last day to drop the class with a W is July 28, 2025. Incomplete grades (IN) are rarely assigned. The IN grade may only be justified in exceptional cases such as student illness or a personal tragic event that occurs in the semester. Visit https://classes.usc.edu/term-20252/classes/ee/ for more information and any important dates.

Textbook

Fundamentals of Layout Design for Electronic Circuits
Jens Lienig, Juergen Scheible
2020, 306 pages, Springer International Publishing
ISBN 978-3-030-39283-3, eBook ISBN 978-3-030-39284-0

Instructor Information

Susie Schober
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Office Hours: Tuesday and Thursday after class in OHE230 2:05pm-3:00pm

Teaching Assistant (To be updated for Summer 2025)

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Please note: Our TAs will be in-class helping out in-person in lieu of office hours. Please post all questions for your circuit and layout projects directly on the class discussion board in Brightspace and the TA, instructor, and students can all participate in helping find solutions.

The EE505 website is located on brightspace.usc.edu.

Following this class, each Spring, the USC ECE department will offer EE599: Analog, Mixed Signal, and RF IC Measurements for students who would like to receive their ICs back from fabrication and test their circuits. As mentioned above, the actual tapeout is dependent on fabrication schedules and completion of the full design, and generally happens in the Fall semester so that the packaged chips can be tested in the Spring. Taking EE505 with EE599 is not required, but recommended as both classes can be taken stand-alone or together.

Please note that all dates listed in this syllabus are tentative and may be updated by the instructor.