University of Southern California
Viterbi School of Engineering
Ming Hsieh Department of Electrical Engineering

EE202L – Linear Circuits (4.0 units)
Course Syllabus
Spring 2025

Lecture:

Tuesday and Thursday
8:00am-9:50am (Professor Maby) and 10:00am-11:50pm (Professor Schober)
OHE230

Lab:

Monday (4:00-5:50pm or 6:00-7:50pm) in OHE230

Instructors:

Professor Edward Maby
Email: maby@usc.edu
Office Hours: Tuesday 10:00am-11:30am
Office: PHE630

Professor Susie Schober
Email: schober@usc.edu
Office Hours: Tuesday and Thursday 1:50pm-2:50pm in OHE230/240
Office: PHE628

Abstract

EE202L is a fundamental electronics course which covers the analysis and design of linear circuits and networks. The course consists of a theoretical lecture and a laboratory component.

Topics included in this class include: lumped circuit elements; network equations; zero-input and zero-state responses; sinusoidal steady-state analysis; impedance; resonance; network functions; power concepts; transformers; and Laplace transforms.

EE202L is a gateway course. Students who are interested in modern electronic circuits will want to consider EE348L, EE354L, EE447L, EE448L, EE477L, EE505ab, EE536ab, and E631/2 as courses leading to a strong background in digital, analog, mixed-signal integrated circuits. Such engineers continue to be in great demand.

Course Administration

EE202L is a 2-hour lecture format class taught on Tuesdays and Thursdays and led by the instructors. The lab is held on Mondays and conducted by the teaching assistant(s) with the course producers.

The co-requisite is MATH245.

The last day to drop the class without a W grade is February 28, 2025, without a refund (January 31, 2025, with a refund). The last day to drop the class with a W is April 11, 2025. (Reference: https://classes.usc.edu/term-20251/registration-calendar/) Incomplete grades (IN) are rarely assigned. The IN grade may only be justified in exceptional cases such as student illness or a personal tragic event that occurs after the twelfth week of the semester.

The EE202L grade is based on the following components:

Midterm Exam #1 (February 24, 2025): 20%
Midterm Exam #2 (March 31, 2025): 20%
Circuit Boot Camp: 10%
Homework: 10%
Laboratory/Projects: 15%
Final Exam (University Schedule): 25%

Historically, the average grade for EE202L is a B following the application of a "curve." Homework conditions borderline grades. Notwithstanding, the instructor is prepared to accept a higher average if the class does exceptionally well—for example, a total class average score of 99/100 is clearly an A.

Apart from numerical grades for the final exam, grades will be posted by May 6, 2025. It is the student's responsibility to verify (and possibly contest) these grades **before** the final exam. **Once assigned, a letter grade will not be changed except for grossly erroneous circumstances.**

Try not to miss class! Students who are regularly absent invariably receive poor grades. The instructor has no reservations about compiling homework assignments and exams that are predicted, in part, on material discussed in class but not in assigned readings. All labs assigned must be completed to receive a course grade; the TA will make one lab session dedicated to making up any labs if not completed in time; **make-up labs will have a -10% penalty if completed after the due date at any time before the end of the semester** (please see the teaching assistant for obtaining partial credit if needed).

Make-up exams and finals are not available. Exams and finals are only completed on the day set by the instructor, in class with the other students; no earlier or later. If you are absent during an examination, you will receive a grade of zero unless you have a valid reason for your absence, **and you have discussed it with the instructor prior to the exam.** In the event of an excuse from a midterm, a weighted final exam score will replace the missing score. If you cheat during an exam, you will receive a grade of F in the course and you will be reported to the Office of Student Conduct for further disciplinary action. If you have special accommodations by the university, please discuss your options prior to the exam with the instructor.

Homework and the Bootcamps are crucial in EE202L, since it provides much needed practice in analytical techniques, it is a good measure of whether you understand the fundamental concepts, and it is a prerequisite for good performance on course exams. If your weighted course average places you on the borderline between two letter grades, a poor homework average will significantly increase the probability of a lower grade. Also, **if a Homework or Bootcamp is turned in after the due date, a -10% penalty will be applied per day it is late)**. Please contact/email the teaching assistant if this occurs so they can accept your homework and grade it. Remember that Homework conditions borderline grades.

You are encouraged to use computer analysis tools such as PSpice, HSpice, LTSpice to check homework. Be sure not to use the computer as a "crutch." You will not have access during exams.

Textbook:

The Analysis and Design of Linear Circuits, Tenth Edition
R. Thomas, A. Rosa, G. Toussaint
Wiley

Brightspace.usc.edu:

Lecture Slides
Supplementary Notes and Handouts
Spice Documentation

Teaching Assistants:

Rifat Shahriar
rshahria@usc.edu

Dingzhou Cui
dingzhou@usc.edu

Nishat Hiramony
hiramony@usc.edu

Office Hours: TBA on Brightspace

Course Producers:

Melissa Shun (Head CP)
mshun@usc.edu

Full Course Producer list will be updated on Brightspace.
One-on-One Mentoring Hour with Zoom Link: TBA on Brightspace

EE Instructional Lab Manager:

Nathan M. Timpke
timpke@usc.edu

EE202L - Tentative Schedule - Spring 2025

Week	Monday (Lab)	Tuesday	Thursday
1 - 13 Jan.	No Lab	Electrical Networks Kirchhoff's Laws, Ohm's Law	Series/Parallel Resistance Voltage/Current Dividers
2 - 20 Jan.	MLK Day - No Lab	Superposition Source Substitutions, SPICE	Node and Loop Equations Bootcamp #1 Due
3 - 27 Jan.	Lab #1 DC Measurements	Thevenin/Norton Equivalents	Review - Practice Problems Bootcamp #2 Due
4 - 3 Feb..	Lab #2 Thevenin Analysis	Op-Amps	R-2R DAC Bootcamp #3 Due
5 - 10 Feb.	Lab #3 R-2R DAC	Comparators Flash/Pipeline ADCs	Capacitors, Integrating ADC HW #1 Due
6 - 17 Feb.	Presidents' Day - No Lab	Algorithmic ADCs Conversion Errors	First MT Review HW #2 Due
7 - 24 Feb.	Midterm Exam #1	First-Order Circuits (Time Domain), 555 Timer	555 Timer HW #3 Due
8 - 3 Mar.	Lab #4 Transient Analysis	Sinusoidal Steady State Impedances	First-order Filters HW #4 Due
9 - 10 Mar.	Lab #5 Filter Analysis	Second-Order Filters	Active Filters HW #5 Due
	SPRING BREAK		
10 - 24 Mar.	Lab #6 Bandpass Filter	Second-Order Circuits (Time Domain)	Second MT Review
11 - 31 Mar.	Midterm Exam #2	Laplace Transforms	Notch Filter Design HW #6 Due
12 - 7 Apr.	Notch Filter Design	Laplace Transform Analysis	Board Design HW #7 Due
13 - 14 Apr.	Board Design	Guitar Construction	Guitar Construction HW #8 Due
14 - 21 Apr.	Guitar Construction	Guitar Construction	Guitar Construction
15 - 28 Apr.	Board Stuffing	Project Integration and Test	Final Review