

**University of Southern California
Viterbi School of Engineering
Ming Hsieh Department of Electrical Engineering**

**EE599 – Analog, Mixed Signal, and RF Integrated Circuit Tapeout
Course Syllabus
Summer 2024**

Abstract

EE599 is an introductory tapeout class. Complete systematic tape-out flow including schematic design, simulation, layout and post-layout verification of analog, mixed-signal or radio-frequency (RF) integrated circuits (IC) is covered. However, the course is mainly taught with an emphasis in analog design, combined with digital and RF. The goal in EE599 is to participate in an actual tapeout of your work by submitting for fabrication so that it may be tested in the future. We plan to use the TSMC 180nm CMOS process design kit (PDK) along with Cadence Design Tools at USC.

Course Administration

EE599 is a 2 hour “studio” format on Tuesdays and Thursdays in which lecture is taught by the instructor on Tuesdays and Thursdays are held as an in-class workshop time with student project updates where help with the chip layout is received, all in the same setting. All classes meet in OHE230 from 12:00-2:05pm. The class will be recorded on Zoom via Blackboard so students can review the lecture and participate remotely as needed. The prerequisite is EE536a and/or EE477L (please see your courses advisor for clearance).

The EE599 grade is based on the following components:

Project 1 (Due: TBD): “Differential” aka “Balanced” Transimpedance Amplifier (TIA): 20%

Project 2 (Due: TBD): Fully Differential Operational Amplifier with Digital Clocking (OpAmp): 20%

Project 3 (Due: TBD): Ring Voltage Controlled Oscillator (VCO) w/Resistor, Capacitor, and Inductor Cross-Coupling for kicks: 20%

Project 4 (Due: TBD): Custom Analog Pads and Pad Ring (with above Circuitry): 20%

End of the Semester Project Team Presentation/Design Review on Zoom (Due: TBD – In person or pre-recorded for the class is fine and presented) and Writeup (Due: TBD – No class this day, just submission of the final writeup of all your team’s work): 20%

For each of the 4 Projects, this will be a “soft” deadline with the completion of the given circuit blocks and sizing assigned to you in class. You can upload your design rule check (DRC) and layout versus schematic (LVS) clean initial Graphic Design System (gds), schematics, and any simulation zipped files to Blackboard where the TA will create a Blackboard submission site for each project to be reviewed by the professor.

For the final end of the semester project presentation, writeup, and submittal, this will be a “hard” deadline, where you will be instructed how we will be placing these projects together as a class into the final ICs to be submitted for Tapeout after the end of the semester, along with other checks like antenna and electric rule checks (ERC) which must be completed by the teams with the simulation (as needed) of the circuits to verify they are working as planned and, of course, the final submittal of the schematic, gds, simulation files for preparation of the Tapeout.

We will work in teams of 2 in order to complete 4 main assigned IC layout projects, which will be explained further in class, in that the circuit design and basic sizing will be given to you and your work as a team is to replicate the schematic in Cadence and build the physical design (i.e. layout) of the given blocks which will be placed in an IC for fabrication once all rule checks have been verified as clean. It is expected that you know how to characterize and simulate basic analog circuits in Cadence via EE536a, as these can supplement your project deadline submittals.

If you are a distance student, you can log on to Zoom to watch/participate during the class time (and at other times if needed) along with teaming with an in-class student so that you can work together to stay up-to-date. It is your responsibility to make sure you stay in contact with your teammate and the professor in getting your projects completed if you choose to do this and work remotely.

The TA and instructor will help monitor a Blackboard EE599 discussion board where you can post any questions you have regarding the projects, so that everyone, including all students can help answer any issues that may arise with Cadence and the pdk as we go together through the semester. The goal is to work as a team both with a partner and the whole class to successfully reach a Tapeout in the short 8 weeks we are given for the summer session and this requires helping each other. We ask that you first post in the discussion board to ask any questions or share information you may encounter that can help others here instead of emailing directly the TA and Professor if it has to do with work on the assigned projects.

Apart from numerical grades for the assignments above, final class letter grades will be posted on Blackboard by TBD. It is the student’s responsibility to verify (and possibly contest) these grades **before** the grade deadline on TBD. **Once assigned, a letter grade will not be changed except for grossly erroneous circumstances.**

The last day to drop the class without a W grade is TBD, without a refund (TBD, with a refund). The last day to drop the class with a W is TBD. Incomplete grades (IN) are rarely assigned. The IN grade may only be justified in exceptional cases such as student illness or a personal tragic event that occurs in the semester. Visit <https://classes.usc.edu/term-2024/classes/ee/> for more information.

Textbook

Fundamentals of Layout Design for Electronic Circuits

Jens Lienig, Juergen Scheible

2020, 306 pages, Springer International Publishing

ISBN 978-3-030-39283-3, eBook ISBN 978-3-030-39284-0

Instructor Information

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Please note: Our TA will be in-class helping out in-person in lieu of office hours. Please post all questions for your circuit and layout projects directly on the class discussion board in Blackboard and the TA, instructor, and students can all participate in helping find solutions.

The EE599 website is located on blackboard.usc.edu.

Following this class, each Spring, the USC ECE department will offer EE599: Analog, Mixed Signal, and RF IC Measurements for students who would like to receive their ICs back from fabrication and test their circuits.