12/24/2023 (Undergraduate students, who got an "A" or an "A-" grade in their EE354L, do not have to submit HW#1)

Dear EE457 students of Spring 2024,

Welcome to EE457! Hope you all had a safe and enjoyable winter vacation!

About two-thirds of the students in EE457 are usually graduate students doing their first semester at USC. If you are one of them, then welcome to USC and to the ECE Department too!

First things first! Please check that you do not have any time conflicts with the three exams as there are no make-up exams. EE457 exams are design exams and are 3 hours long.

Extract from the syllabus .pdf .docx:

Quiz (~11%): Friday, Feb. 9, 2024, 05:00 PM - 08:00 PM PST
Midterm (~25%): Friday, Mar. 22, 2024, 05:00 PM - 08:00 PM PST
Final Exam (~34%): Wednesday, May 8, 2024, 03:30 PM - 06:30 PM PST **Please check**
Official slot of 4:30-6:30PM extended by an hour

Web links: I hope I have renewed all web links. But in case you come across any non-working web link, please inform me. Also use the following note to fix it by yourselves.
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The ee457 documents are on two servers. 1. A few documents are on the ee server (links starting with ee https://ee-classes.usc.edu/ or starting with ece https://ece-classes.usc.edu/ (both are equivalent)) (if the link starts with http://, then change it to https://). 2. Most other documents are on the scf (student computing facility) server. In Fall 2022, we moved the ee457 scf UNIX course directory from an old server (aludra.usc.edu) to a new server (viterbi-web.usc.edu). We corrected web links in various documents progressively. We replaced the earlier prefix http://www-classes.usc.edu/engr/ee-s/ in every web link to the newer prefix https://viterbi-web.usc.edu/www-classes/engr/ee-s/ Similarly, we replaced an earlier prefix reading http://ee-classes.usc.edu/ by https://ece-classes.usc.edu/ . If you find a web link which has not been updated, I appreciate it very much if you report the old link to me in an email to me.
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First three weeks are important to all EE457 students who have not taken EE354L (previously called EE254L/EE201L).

EE457 (Computer Systems Organization) course provides you with foundation material needed to proceed to higher courses such as EE557, EE577a, EE533, and EE560.

If you are a continuing undergraduate student who did not get an A in your EE354L, the rest of this document applies to you also.

The prerequisite course, EE354L (previously called EE254L or EE201L), has been waived for the graduate students but our experience over the last 30 years tells us that most graduate students do not come with adequate introduction to logic design necessary for this course. So, I am providing some make up material which helps them to "survive" in the first three weeks of this course. This material is not difficult, but it is not too easy either. It is not quite intuitive, so it takes substantial time and effort (and creativity and imagination). So, I ask the graduate students to put in at least **30 hours** (in the days leading to first week of classes) preparing for EE457. We have assignments due from the 2nd week of classes and it will be overwhelming if you do not put in time to make up for the lack of prerequisite knowledge. Due dates can be seen in this calendar.

Detailed information about what you should do before the start of the semester is given in this document "Study plan for the first three weeks" (provided in two formats):
pdf: https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_Sp2024_exams/EE457_Study_Plan_for_first_3_weeks.pdf
docx: https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_Sp2024_exams/EE457_Study_Plan_for_first_3_weeks.docx
This page is the first page of the above document.

It will be great if you go through most of the items provided below and actually complete the HW#1 and HW#1B. and start working on HW#1C (EE457_prelude_to_HW1C.pdf & EE457_HW1C_3pages_assignment.pdf). Undergraduate students, who got an "A" or an "A-" grade in their EE354L, do not have to do HW#1 . They need to submit a "Waiver Note". Please see HW#1 posting on D2L. However, they need to do HW#1B and HW#1C.

Best wishes,

Gandhi Puvvada

What do I want the graduate students to do in the first three weeks:

Please seek help whenever you need from the teaching team, but not through email. If it is a very simple/short question, you can use Piazza, but otherwise, please come and meet us well prepared to ask your question. After every lecture, go through the material covered in the lecture and prepare your list of questions to ask.

1. Please install several tools including Modelsim on your laptop (windows laptop) as per the following note.
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_tools/EE457_README_first.pdf
Use the following userID and 10-digit StudentID to access the following installation guide and to download the installation files for Modelsim SE 10.6e

User name: ttrojan
10-digit ID for Password: 1010101010
https://ece-classes.usc.edu/ee201/0lO100ooll11/f0r_UsC_oN1y/MSim_SE_10.6e/ModelSim_SE_10_6e_Installation_by_USC_students.pdf
https://ece-classes.usc.edu/ee201/0lO100ooll11/f0r_UsC_oN1y/MSim_SE_10.6e/ModelSim_SE_10_6e_Installation_by_USC_students.pdf

If you do not have a Desktop/Laptop running windows 10 or 11, please buy one (or consider the alternatives stated at the bottom of EE457_README_first.pdf).

2. In the first week of classes, we cover the following 6 topics. However, I want you to watch the 6 short videos on the 6 topics at the following web directory before the first day of classes.
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/ .
(**a**) DPU and CU design (**b**) Mealy machine example -- Divider Design (**c**) Data registers -- clocking and controlling (**d**) Loop Counter Incrementation and Terminal Value Checking (**e**) ME (Mutually Exclusive) and AI (All Inclusive) rules in designing a state diagram (**f**) State diagram Design examples

3. Notice that, while HW#1 and HW#1B are assigned, the HW#1A is provided with solution to serve as a practice item. It has four problems. I suggest that you do at least the 2nd problem (Make A close to B) and verify your work with the solution. Come to us if you do not understand the solution. Do not be lazy. Design takes time and effort to learn.

4. Then start working on HW#1 followed by HW#1B.

5. Watch the 6 Verilog lectures listed later in this document.

Complete the Verilog code for the HW#1A 2nd problem (Make A close to B) and verify. This is for practice only. It is worthwhile to go through the following procedural steps to simulate and submit:
Procedural steps illustration (from EE201L):
https://viterbi-web.usc.edu/www-classes/engr/ee-s/201/RTL_coding/ee201_RTL_exercises_Sp2010/EE201L_Introducing_the_procedure_associated_with_HW8A.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/201/RTL_coding/ee201_RTL_exercises_Sp2010/EE201L_Introducing_the_procedure_associated_with_HW8A.avi
Note: If you do not see picture when playing the *.avi* video files, then you need to install the TSCC codec from https://www.techsmith.com/codecs.html

6. Start working on the lab 1 of EE457 (Min/Max Finder -- 6 parts, but only 4 parts will be assigned).

If you put in goo effort, you will feel good that you are able to follow the first week of lectures (which are covered at a fast rate).

First week's lecture notes and webcasts reviewing EE201L material (.pdf files for slides + .avi or .wmv files for video):

You need to install on your PC TechSmith TSCC Codec to view .avi video files.

1. Chapter #1 Intro.

https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/ee457x1_Chapter1_microarchitecture.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/1_EE457_Chapter1_microarchitecture.avi

2. DPU and CU

https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/ee457x2_DPU_CU.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/2_DPU_CU.wmv

3. Mealy machine example -- Divider Design

https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/ee457x3_Moore_Mealy_Divider.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/3_Divider_Mealy_example.avi

4. Data registers -- clocking and controlling

https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/ee457x4_Data_Registers.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/4_Data_Registers_with_Data_Enable.avi

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5. Loop Counter Incrementation and Terminal Value Checking

https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/EE457x5_P1_loop_counter.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/EE457x5_P2_loop_counter_example_doubling_A.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/EE457x5_P3_loop_counter_ee102_midterm1_Sp2005_Q4_question_and_solution.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/EE457x5_P3_loop_counter_ee102_midterm1_Sp2005_Q4_transparencies.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/5_Loop_Iteration_Counter.avi

6. ME (Mutually Exclusive) and AI (All Inclusive) rules in designing a state diagram

https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/ee457x6_P1_mutually_exclusive.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/ee457x6_P2_ME_AI_tables.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/6_Mutually_Exclusive_All_Inclusive.avi

7. State diagram Design examples

OLD: ~~https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/ee457x7_State_Diagram_Design_examples.pdf~~
OLD: ~~https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/7_State_Diagram_Design_examples.avi~~
NEW: https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/EE354_HW1.pdf
NEW: https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/EE354_HW1_sol.pdf
<= Please do not share with the current EE354L students
NEW: https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_first_lecture/EE354L_HW1_introduction.mp4

EE457 HW#1 (Due: calendar)

Undergraduate students, who got an "A" or an "A-" grade in their EE354L, do not have to submit HW#1 (ee457_hw1_r1.pdf) .
However, they need to submit a HW#1 Waiver application. Please see HW#1 posting on D2L

Homework #1 (16 pages) Revised in Fall 2020
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_Homeworks/HW1/ee457_hw1_r1.pdf

On-campus students will be given hard-copies of the assignment in the first week of classes.

State Diagram design: If you are new to this topic, first go through these (.pdf .avi).

Additional help on the first 10 pages (first two questions related to datapath design) of this homework:
The first 10 pages of this homework are from the EE101/EE354L homework on datapath design for which solution and webcast are provided below. Do not just copy the solution. Understand the solution. If you are new to this topic, please watch the webcast also.
EE101 items on datapath: ee101_hw_on_datapath.pdf ee101_hw_on_datapath_sol.pdf
ee101_hw_on_datapath.mp4

Q#3 on pages 11 and 12 assumes that everyone has gone through the Q#2 of HW#1A (the next page provides information about the HW#1A and its solution).

HW#1A (for practice only, not for submission)

This HW#1A is an additional practice for graduate students who did not take EE354L (previously called EE254L/EE201L) here at USC. You do not need to submit this.

https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/EE457_HW1A/EE457_HW1A_EE201L_RTL_Exercises.pdf

Additional help on next page.

Solution: Please do not show this to the EE354L students as it is an assignment in their course:

https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/EE457_HW1A/DO_NOT_SHOW_TO_EE354L_students/

Help on HW#1A (for practice only, not for submission)

Watch these webcasts one at a time and then complete the state diagram. Check with the solution.

Right-click on the video file and download it. Do not stream the videos. The server is not meant for video streaming.
If the video does not play on your computer, then you need to install TSCC codec from TechSmith. TechSmith links are provided below.
https://www.techsmith.com/download.html
https://www.techsmith.com/tscc/tscc.exe

1. The last question (Q#4) of EE201L quiz of Spring 2010
Q#4 Convert Inches to Feet and further to Yards
https://viterbi-web.usc.edu/www-classes/engr/ee-s/201/EE201L_Sp2010_Exams/ee201_Quiz_Sp2010_Pages_9_10_DataPath_Inches_Feet_Yards_lec_mht.pdf
.mp4 video file
Right-click on the .mp4 file link below and select "Save Target as" to download.
https://viterbi-web.usc.edu/www-classes/engr/ee-s/201/EE201L_Sp2010_Exams/ee201_Quiz_Sp2010_Pages_9_10_DataPath_Inches_Feet_Yards.mp4
https://viterbi-web.usc.edu/www-classes/engr/ee-s/201/EE201L_Sp2010_Exams/ee201_Quiz_Sp2010_Pages_9_10_DataPath_Inches_Feet_Yards_sol.pdf

2. The **first 3** questions of the EE201L RTL coding exercises:

https://viterbi-web.usc.edu/www-classes/engr/ee-s/201/RTL_coding/ee201_RTL_exercises_Sp2010/

The assignment (only the **first 6** pages)
https://viterbi-web.usc.edu/www-classes/engr/ee-s/201/RTL_coding/ee201_RTL_exercises_Sp2010/EE201L_RTL_exercises_Spring2010.pdf

Q#1 Largest Number Divisible by 7
https://viterbi-web.usc.edu/www-classes/engr/ee-s/201/RTL_coding/ee201_RTL_exercises_Sp2010/EE201L_RTL_exercises_Spring2010_Q1.pdf
.wmv file:
Right-click and select "Save Target as" to download EE201L_RTL_exercises_Spring2010_Q1.wmv
https://viterbi-web.usc.edu/www-classes/engr/ee-s/201/RTL_coding/ee201_RTL_exercises_Sp2010/EE201L_RTL_exercises_Spring2010_Q1.wmv

Q#2 Make A close to B
https://viterbi-web.usc.edu/www-classes/engr/ee-s/201/RTL_coding/ee201_RTL_exercises_Sp2010/EE201L_RTL_exercises_Spring2010_Q2.pdf
.wmv file:
Right-click and select "Save Target as" to download EE201L_RTL_exercises_Spring2010_Q2.wmv
https://viterbi-web.usc.edu/www-classes/engr/ee-s/201/RTL_coding/ee201_RTL_exercises_Sp2010/EE201L_RTL_exercises_Spring2010_Q2.wmv

Q #3 Copying two parts of a sorted array
https://viterbi-web.usc.edu/www-classes/engr/ee-s/201/RTL_coding/ee201_RTL_exercises_Sp2010/EE201L_RTL_exercises_Spring2010_Q3.pdf
.wmv file:
Right-click and select "Save Target as" to download EE201L_RTL_exercises_Spring2010_Q3.wmv
https://viterbi-web.usc.edu/www-classes/engr/ee-s/201/RTL_coding/ee201_RTL_exercises_Sp2010/EE201L_RTL_exercises_Spring2010_Q3.wmv

HW#1B (Due: calendar)

Selected 9 pages (First 6 pages 1/12-6/12 and last 3 pages 10/12-12/12) of the 12-page HW#1B
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_HW1B/ee457_HW1B_r1.pdf

Hard copies will be provided to you in class in the first week.

Help on the last question (Q#1 of EE457 Quiz - Fall 2010) in HW#1B

You may want to review Signed number representation in 2's complement notation. I have provided information below.

Please watch the first 20 minutes (from 00:13:00-00:33:00) of the following lecture (EE457Lx_20123329.wmv):

Chapter 4 Part 1
Signed number representation in 2's complement notation,

Adder/Subtractor design for unsigned numbers and signed number -- overflow detection in each of them

Time: 1 Hour 2 minutes (from 00:13:00-01:15:00)
Open the following directory and download (not stream) the file EE457Lx_20123329.wmv and watch starting at 13-minute point.
https://ece-classes.usc.edu/ee457/ee457_Ch4_P1_Lab3_ALU/Fall2012_Sept_18_20/

Verilog Introduction lectures:

Six lectures (together with slides) were posted at the link below to introduce the essential aspects of Verilog to the EE201L students (and to the graduate students in EE457, who are new to Verilog coding), so that they can get started with using Verilog for completing their labs. The lectures add up to 3 Hours 40 minutes.
https://ece-classes.usc.edu/ee254/Verilog/

0_Verilog_Main_Points_of_the_6_Lectures.pdf (if you already know Verilog, you can view this in lieu of the 6 modules)
https://ece-classes.usc.edu/ee254/Verilog/0_Verilog_Main_Points_of_the_6_Lectures.pdf

1_Verilog_Introduction_mht.pdf
https://ece-classes.usc.edu/ee254/Verilog/1_Verilog_Introduction_mht.pdf
1_Verilog_Introduction.avi (1 H 08 Minutes)
https://ece-classes.usc.edu/ee254/Verilog/1_Verilog_Introduction.avi

2_module_DataTypes_in_Verilog.pdf
https://ece-classes.usc.edu/ee254/Verilog/2_module_DataTypes_in_Verilog.pdf
2_module_DataTypes_in_Verilog.avi (23 minutes)
https://ece-classes.usc.edu/ee254/Verilog/2_module_DataTypes_in_Verilog.avi

3_behavioral_vs_structural_Verilog.pdf
https://ece-classes.usc.edu/ee254/Verilog/3_behavioral_vs_structural_Verilog.pdf
3_behavioral_vs_structural_Verilog.avi (17 minutes)
https://ece-classes.usc.edu/ee254/Verilog/3_behavioral_vs_structural_Verilog.avi

4_Sequential_Statements_in_Verilog.pdf
https://ece-classes.usc.edu/ee254/Verilog/4_Sequential_Statements_in_Verilog.pdf
4_Sequential_Statements_in_Verilog.avi (1 Hour)
https://ece-classes.usc.edu/ee254/Verilog/4_Sequential_Statements_in_Verilog.avi

5_blocking_non_blocking.pdf
https://ece-classes.usc.edu/ee254/Verilog/5_blocking_non_blocking.pdf
5_blocking_non_blocking.avi (56 minutes)
https://ece-classes.usc.edu/ee254/Verilog/5_blocking_non_blocking.avi

6_RTL_coding_style.pdf
https://ece-classes.usc.edu/ee254/Verilog/6_RTL_coding_style.pdf
6_RTL_coding_style.avi (33 minutes)
https://ece-classes.usc.edu/ee254/Verilog/6_RTL_coding_style.avi

EE254L_RTL_coding_style_verilog.pdf
https://ece-classes.usc.edu/ee254/Verilog/EE254L_RTL_coding_style_verilog.pdf
ee254_divider_simple.zip
https://ece-classes.usc.edu/ee254/Verilog/ee254_divider_simple.zip

Lab #1 min/max finder lab (Verilog) (Due: calendar)
Note: The .zip files will be available for download in the second week of classes.

.pdf of the assignment (both in Color and Black_n_White):
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_lab_manual_Fl2010/min_max/ee457_min_max_finder_lab.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_lab_manual_Fl2010/min_max/ee457_min_max_finder_lab_Black_n_White.pdf
Six of the figures in landscape mode for online reading (both in Color and Black_n_White):
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_lab_manual_Fl2010/min_max/ee457_min_max_finder_lab_figures.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_lab_manual_Fl2010/min_max/ee457_min_max_finder_lab_figures_Black_n_White.pdf

Slides (pdf) file used in class lecture
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_lab_manual_Fl2010/min_max/ee457x8_min_max_finder.pdf
Short video and slides explaining part 3 (the four methods M1, M2, M3, and M4)
Note: The Part 3 Method M2 and M4 are cancelled for submission.
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_lab_manual_Fl2010/min_max/min_max_Improved_testbench_part3.pdf
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_lab_manual_Fl2010/min_max/min_max_Improved_testbench_part3.avi

Verilog files for downloading and completing (will be available after the 1st week of classes):
Part 1:
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_lab_manual_Fl2010/min_max/min_max_finder_part1.zip
Part 2:
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_lab_manual_Fl2010/min_max/min_max_finder_part2.zip
Part 3 Method 1:
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_lab_manual_Fl2010/min_max/min_max_finder_part3_M1.zip
~~Part 3 Method 2:~~ cancelled
~~https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_lab_manual_Fl2010/min_max/min_max_finder_part3_M2.zip~~
Part 3 Method 3:
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_lab_manual_Fl2010/min_max/min_max_finder_part3_M3.zip
~~Part 3 Method 4:~~ cancelled
~~https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_lab_manual_Fl2010/min_max/min_max_finder_part3_M4.zip~~

It will be great if you can complete state diagrams on paper for the four parts of Lab 1 (min/max finder) (the first 4 pages of the pdf) before the start of the semester!