EE533 Network Processor Design and Programming
Units: 4
Spring
Lecture: Tues/Thurs, 12:00 – 01:50 P.M.

Location: THH 114

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Teaching Assistant: TBD
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Course Description

This graduate level course teaches students to design, implement, and demonstrate a working custom multiple core Network Processor on a SmartNIC installed in a network security testbed named DETERlab.

The students will have hands-on experience of building a unique custom processor from ground up demonstrating incremental functions of a network specific processor that they will integrate over semester.

The expected result of the final project is a working implementation of a novel networking solution for a real-world problem(s) running on your custom IP router with multiple-core/multiple threaded Network Processors and Hardware Acceleration modules in a realistic network environment within DETER testbed. There is a final course project and the topic must be proposed by thestudents and approved by the instructor. Working as a group is permitted, and a team can consist of 2-3 persons. The grade will be based on the demonstration of working system as well as the final project report that the students will submit at the last day of the finals.

Learning Objectives

After completing this course, students will be able to:
- Design and build custom instruction set architecture for network processor
- Design and integrate hardware components to accelerate multiple threads into a processor
- Integrate application specific hardware accelerators into custom processors
- Translate RISC V assembly code into hardware operations in custom network processor
- Design and assess different multiple core processor architecture for network processing
- Design interrupts, exceptions, and polling mechanisms for networking applications
- Integrate and modify OS level software interface for hardware network interface

Prerequisite(s): EE457
Co-Requisite(s): None
Concurrent Enrollment: None
Recommended Preparation: EE450, experience in Verilog, C/C++ programming language

Course Notes

Copies of all course notes will be posted on Blackboard.

Required Readings and Supplementary Materials

Recent and seminal research publications and survey articles will be used to cover all preparatory materials during the semester. Other supplementary material includes online FPGA tool and Verilog tutorials and videos.

Description and Assessment of Assignments

This course will have will have 11 homework assignments, 10 reading assignments, and a final course project. Homework assignments are designed to incrementally teach the students to get familiar with tools and gain skills necessary to design and build their own custom network processors. The students are required to submit report and a demonstration video for each homework assignment. Reading assignment are designed to expose the students to important core as well as newest relevant concepts behind network processing. The students expected to submit a summary slide deck for each reading assignment. These assignments will be graded based on correct answers and clarity of their explanations. The final course project must include a working hardware system for a specific real-world application. The final course project will begin after all homework assignments are completed. Students will self-organize into teams of 1-3 students and grades will be given to each team. All students are expected to work together.

The final project presentation will be given by the students in the last two lecture times. The final course project demonstration video must be uploaded on to Youtube before the last day of the semester. The final project will be graded based on students progress and successful implementation and demonstration of their proposed tasks.

In addition to these assignment, there will be up to 5 pop quizzes that are designed to test students' understanding of the material discussed during the lectures.

Sample Project

"*Hardware Accelerated Deep Packet Inspection with 8-threaded Dual core Network Processor*": the goal of the project is to develop a custom hardware based IP Router augmented with Dual core 4-way hardware multi-threaded network processor. The network appliance will execute multiple network security software simultaneously as the packets are sent and routed through the router over 1Gbps under DETER network emulation testbed. The following link is an example demonstration video for the class project.

https://www.youtube.com/watch?v=lsnBlNYT0Hk

Grading Breakdown

Assignment	% of Grade
Reading Assignments	10%
Homeworks	30%
3-5 Pop Quizzes	10%
Final Project (Proposal/Presentation/Demo)	50%
TOTAL	100%

Assignment Submission Policy
Assignments will be submitted electronically. Late assignments will be accepted with 50% penalty unless otherwise announced.

Additional Policies
None.

Course Schedule: A Weekly Breakown
All slide deck reports for reading assignments must been submitted on the following Wednesday.
All assignment reports are due Saturday night and the demonstration video is following Monday night

Week-Day	Topics	Readings/Preparation	Homework/Final Project
1-1	Introduction to Network Processor Course	L. White, et al, "An Integrated Experimental Environment for Distributed Systems and Networks", OSDI 2002, Boston, MA, Dec 2002.	DETER Tutorial
1-2	Computer Networks and Internet		
2-1	Measuring Computer Networks	S. J. Lee, P. Sharma, S. Banerjee, S. Basu, and R. Fonseca, "Measuring bandwidth between planetlab nodes," Passive and Active Network Measurement, p. 292–305, 2005.	Advanced DETER Tutorial
2-2	Computer Network Emulation and Network Security using DETERlab Testbed		
3-1	Digital Logic Design, Memory, and Parallel Architectures	Xilinx, "ISE In-Depth Tutorial," http://www.xilinx.com/direct/ise10_tutorials/ise10tut.pdf	Network performance measurement and tuning in DETERlab
3-2	Hardware Description Languages		
4-1	Field Programmable Gate Arrays and Their Microarchitecture	Y. H. Cho, "Optimized Automatic Target Recognition Algorithm on Scalable Myrinet/Field Programmable Array Nodes." 34th IEEE Asilomar Conference on Signals, Systems, and Computers, Monterey, CA, October 2000.	Xilinx ISE/Verilog Tutorials
4-2	Hardware Accelerated Streaming Processing on FPGAs		
5-1	Reconfigurable Hardware in Emulation Environment	Christopher Celio, Palmer Dabbelt, David Patterson, Krste Asanovic, "The Renewed Case for the Reduced Instruction Set Computer: Avoiding ISA Bloat with Macro-Op Fusion for RISC-V," UC Berkeley, July 2016.	Mini-Network Intrusion Detection System Design
5-2	Introduction to SmartNICs		

6-1	Hardware Software Co-designing on NetFPGAs	G. Watson, "NetFPGA: A Tool for Network Research and Education", 2nd Workshop on Architecture Research using FPGA Platforms (WARFP) February, 2006.	Integration of mini-MIDS on to NetFPGA in DETER
6-2	Reference IP Router Design for NetFPGA		
7-1	Pattern Match based Network Monitoring and NetFPGA-specific Accelerators	A. Goodney, S. Narayan, V. Bhandwalkar, and Y. H. Cho, "Pattern Based Packet Filtering using NetFPGA in DETER Infrastructure," First Asia NetFPGA Developers' Workshop, Daejeon, Korea, June 2010.	Development/Demo of custom RISC pipeline project
7-2	Advanced Network Intrusion Detection System and NetFPGA Mini NIDS System		
8-1	Interface via Hardware and Software Registers	P. Crowley, M. E. Fluczynski, J. L. Baer, and B. N. Bershad, "Characterizing processor architectures for programmable network interfaces," in Proceedings of the 14th international conference on Supercomputing, 2000, p. 54–65.	
8-2	Essentials of Computer Architecture		
9-1	Introduction to Network Processors and Their Uses in Modern Cloud Infrastructures	M. Labrecque, J. G. Steffan, G. Salmon, M. Ghobadi, and Y. Ganjali, "NetThreads Routing Edition: Programming NetFPGA with Threaded Software." NetFPGA Developers' Workshop, 2009.	
9-2	Multi-core Processor Architectures and Design and Method of Implementing on NetFPGAs		
10-1	Architecture for Hardware Multiple Threads and 4-Thread Design for NetFPGA Network Processor Designs	McKeown, N. et al, "OpenFlow: enabling innovation in campus networks", ACM SIGCOMM Computer Communication Review, vol. 38, New York, NY, April 2008.	
10-2	Advanced Network Processor Technologies		
11-1	SmartNICs for the Next Generation Cloud	Moscola, J. et al., "Reconfigurable Content-based Router Using Hardware-Accelerated Language	

11-2	Integration with Interrupts and Exceptions and their Uses in NetFPGA	Parser", ACM Transaction on Design Automation of Electronic Systems on Demonstrable Software Systems and Hardware Platforms, Volume 13, Number 2, April 2008.	
12-1	Commodity Network Processors	Y. Le et al., "UNO: Uniflying host and smart NIC offload for flexible packet processing," in Proceedings of the 2017 Symposium on Cloud Computing, 2017, pp. 506–519.	
12-2	Advanced Uses of Smart Network Interface Cards		
13-1	Custom Network Processor	A. Muhammad, G. Zervas, and R. Forchheimer, "Resource allocation for space-division multiplexing: Optical white box versus optical black box networking," Journal of Lightwave Technology, vol. 33, no. 23, pp. 4928–4941, 2015.	
13-2	Introduction to White Boxes		
14-1	Software Defined Network on Smart NICs and White Boxes	S. Azodolmolky, P. Wieder, and R. Yahyapour, "SDN-based cloud computing networking," in 2013 15th international conference on transparent optical networks (ICTON), 2013, pp. 1–4.	
14-2	Network Processing in Mobile Embedded Systems		
15-1	Future of the Computer Networking	P. Molinero-Fernández, N. McKeown, and H. Zhang, "Is IP going to take over the world (of communications)?," ACM SIGCOMM Computer Communication Review, vol. 33, no. 1, pp. 113–118, 2003.	
15-2	Computer Networks HW/SW Engineering		

Statement on Academic Conduct and Support Systems

Academic Conduct:

Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in SCampus in Part B, Section 11, "Behavior Violating University Standards" policy.usc.edu/scampus-part-b. Other forms of academic dishonesty are equally unacceptable. See additional information in SCampus and university policies on Research and Scholarship Misconduct.

Students and Disability Accommodations:

USC welcomes students with disabilities into all of the University's educational programs. The Office of Student Accessibility Services (OSAS) is responsible for the determination of appropriate accommodations for students who encounter disability-related barriers. Once a student has completed the OSAS process (registration, initial appointment, and submitted documentation) and accommodations are determined to be reasonable and appropriate, a Letter of Accommodation (LOA) will be available to generate for each course. The LOA must be given to each course instructor by the student and followed up with a discussion. This should be done as early in the semester as possible as accommodations are not retroactive. More information can be found at osas.usc.edu. You may contact OSAS at (213) 740-0776 or via email at osasfrontdesk@usc.edu.

Support Systems:

Counseling and Mental Health - (213) 740-9355 – 24/7 on call
studenthealth.usc.edu/counseling
Free and confidential mental health treatment for students, including short-term psychotherapy, group counseling, stress fitness workshops, and crisis intervention.

National Suicide Prevention Lifeline - 1 (800) 273-8255 – 24/7 on call
suicidepreventionlifeline.org
Free and confidential emotional support to people in suicidal crisis or emotional distress 24 hours a day, 7 days a week.

Relationship and Sexual Violence Prevention Services (RSVP) - (213) 740-9355(WELL), press "0" after hours – 24/7 on call
studenthealth.usc.edu/sexual-assault
Free and confidential therapy services, workshops, and training for situations related to gender-based harm.

Office for Equity, Equal Opportunity, and Title IX (EEO-TIX) - (213) 740-5086
eeotix.usc.edu
Information about how to get help or help someone affected by harassment or discrimination, rights of protected classes, reporting options, and additional resources for students, faculty, staff, visitors, and applicants.

Reporting Incidents of Bias or Harassment - (213) 740-5086 or (213) 821-8298
usc-advocate.symplicity.com/care_report
Avenue to report incidents of bias, hate crimes, and microaggressions to the Office for Equity, Equal Opportunity, and Title for appropriate investigation, supportive measures, and response.

The Office of Student Accessibility Services (OSAS) - (213) 740-0776
osas.usc.edu

OSAS ensures equal access for students with disabilities through providing academic accommodations and auxiliary aids in accordance with federal laws and university policy.

USC Campus Support and Intervention - (213) 821-4710
campussupport.usc.edu
Assists students and families in resolving complex personal, financial, and academic issues adversely affecting their success as a student.

Diversity, Equity and Inclusion - (213) 740-2101
diversity.usc.edu
Information on events, programs and training, the Provost's Diversity and Inclusion Council, Diversity Liaisons for each academic school, chronology, participation, and various resources for students.

USC Emergency - UPC: (213) 740-4321, HSC: (323) 442-1000 – 24/7 on call
dps.usc.edu, emergency.usc.edu
Emergency assistance and avenue to report a crime. Latest updates regarding safety, including ways in which instruction will be continued if an officially declared emergency makes travel to campus infeasible.

USC Department of Public Safety - UPC: (213) 740-6000, HSC: (323) 442-120 – 24/7 on call
dps.usc.edu
Non-emergency assistance or information.

Office of the Ombuds - (213) 821-9556 (UPC) / (323-442-0382 (HSC)
ombuds.usc.edu
A safe and confidential place to share your USC-related issues with a University Ombuds who will work with you to explore options or paths to manage your concern.

*Occupational Therapy Faculty Practice - (323) 442-33*40 or otfp@med.usc.edu
chan.usc.edu/otfp
Confidential Lifestyle Redesign services for USC students to support health promoting habits and routines that enhance quality of life and academic performance.