EE552 Asynchronous VLSI Design

Units: 4
Spring 2021
Lecture: T/Th: 9am-11:50am (1hr 50min x 2)
Discussion: Friday: 1pm-1:50pm.

Location: TBD

Instructor: Peter A. Beerel
Office: EEB 350
Office Hours: Wed: 9:00am-10:00am
Contact Info: pabeerel@usc.edu. I will try to answer all emails within 48 hours.

Teaching Assistant: Yuke Zhang
Office: TBD
Office Hours:
Contact Info: TBD

Course Description

This course will introduce students to the field of asynchronous VLSI design with a focus on its application in large-scale VLSI designs.

Asynchronous design has been an active area of research for the past 30 years. Many fundamental techniques, asynchronous design styles, and computer-aided-design flows have been developed that target energy-efficient computing, network on chips, globally-asynchronous locally synchronous (GALS) design. Specific application targets that will be discussed included neuromorphic computing, machine learning, and radiation-hardened design.

Topics covered in this course will include traditional hazard-free logic design and state assignment in fundamental mode asynchronous finite state machines, along with more modern quasi-delay-insensitive and bundled-data-based design styles and associated testing techniques. We will cover CAD topics of performance analysis and pipeline optimization as well as the pervasive issues of metastability, synchronizers, and crossing-clock boundaries.

This course will study the various design styles and provide students with hands-on experience with some of the current state-of-the-art asynchronous tools. In particular, System Verilog will be used to model and design asynchronous architectures. A class project will enable students to study asynchronous architectures and design with one of several promising design styles targeting a machine learning accelerator.

Learning Objectives and Outcomes

Understand channel-based communicating sequential processes and their SystemVerilog models
Learn quasi-delay-insenstive and bundled-data asynchronous design styles
Proficiency in performance analysis of asynchronous design, including Petri-net models and slack-matching
Understand metastability and learn several design techniques to mitigate its effect
Understand network on chip fundamentals comparing asynchronous and synchronous solutions
Evaluate application of asynchronous design in GALS and radiation-hardened design
Evaluate application of asynchronous design in neuromorphic and machine learning acceleration

Prerequisite(s): EE477
Co-Requisite(s): None
Concurrent Enrollment: None
Recommended Preparation: EE457 or other basic course in computer architecture. Basic software programming and scripting experience desired.

Course Notes

Copies of all course notes will be posted on Blackboard.

Required Readings and Supplementary Materials

The course will be based on the book *Asynchronous VLSI – A Designer's Perspective*, by Beerel, Ozdag, and Ferretti, Cambridge University Press, 2010 as well as recent research publications and survey articles. Supplemental materials will be provided in the lectures as well as in the discussion sessions.

Description and Assessment of Assignments

This course will have a midterm, final, and class project. There will also be 6-8 homework assignments. The class project will begin after the midterm and be broken into several phases. Students will self-organize into teams of 1-4 students and grades will be given to each team. It will include a required report (at least 10 pages) and class presentation that will be graded for both content and clarity. All students are expected to participate in the class presentation which is expected to be ~8 minutes long. If needed due to time constraints some presentations will be held outside of normal class times. Homeworks are due one week after assigned, unless explicitly stated otherwise.

Sample Project

Motivated by industrial large-scale spiking neural networks TrueNorth and Loihi, we propose as a class project to model and implement a machine learning accelerator using a 2-D array of processing elements in System Verilog. Unlike TrueNorth and Loihi, however, we will target more traditional machine learning algorithms (e.g., convolutional neural networks) and include a discussion of how CNNs have been mapped to asynchronous Spiking Neural Networks (SNNs). This will focus the class towards the application of this technology in a domain that is quite relevant to todays chip designers. The class project will involve modeling the behavior of the neurons and associated network on chip as well as implementing components in an asynchronous bundled-data design style. The project will thus include aspects of architecture, micro-architecture, circuit design, modeling and verification. We will be using a collection of industrial language and tools (System Verilog) as well as academic scripts to facilitate the design.

The class project has four stages

- Stage 1: Team formation and project definition. The project description will contain a description of a baseline design as well as several opportunities for enhancements. Teams will self-form and describe their intended design. Teams can be from 1 to 4 people. Teams of smaller size will be expected to do a baseline design. Teams of larger size will be expected to add additional features to the design.
- Stage 2: Project Midterm report. Teams are expected to submit a midterm report with most of the architecture and micro-architecture design completed. This will provide an opportunity for the teaching team to give feedback to each team individually.

- Stage 3: Class presentation. Each team will give a 8-10 minute presentation in the last week of classes, typically no more than 12 PPT slides. Each team member should present. Teams of larger size (3 or 4 people) can take an additional 2 minutes.
- Stage 4: Final report. The final report is due on the last day of classes (not including wellness days). It should incorporate any last minute design fixes and feedback from the class presentation.

The grading of the class project is defined by the following rubric:

- Project quality is defined by
    - tasks completed (e.g., architecture design and description, testbench design, high-level SystemVerilogCSP design, gate-level design)
    - design verification – strong testbench with golden model
    - design analysis – detailed study of throughput, latency, bottlenecks, design comparisons, etc…
    - changes in plan from proposal and the rationale -- this should include things that did not work out.
    - novelty & significance: what did you add to the resources that you started with? How challenging was your project objective? (team size will be considered)
- Project Presentation (20 points)
    - project quality (10) -- as defined above and conveyed by your presentation
    - presentation quality (10)
        - slide quality
        - presentation organization
        - presentation delivery
        - Q&A session
        - NOTE: one score for the entire group (typically), but all members must present
- Project Final Report (80 points)
    - project quality (50) -- as defined above and conveyed by your report
    - report quality (30)
        - Clearly stating project objectives
        - Clearly describing proposed architecture and micro-architecture
        - Clear description of testbench and test cases
        - Clear description of analysis of design (performance, latency, throughput, tradeoffs)
        - Clearly stating accomplishments (see quality above)
        - Clearly describing future work (if you were to continue on this or if another team picked up from where you left off)
        - Proper references (included any figures you did not create)

Grading Breakdown

Assignment	**% of Grade**
Homework (~8 assignments)	20%
Midterm	25%
Project	25%
Final	30%
TOTAL	100%

Assignment Submission Policy
Assignments will be submitted electronically. Late assignments will be accepted with penalty, 5% per day, unless otherwise announced.

Additional Policies
None.

Course Schedule: A Weekly Breakdown

Week	Topics/Daily Activities	Readings / Homework	Discussion Section	HW Assignments / Project Due Dates
1 **1/10**	Introduction to VLSI and Async design and applications. Course goals & logistics.	**Required**: *Chapter 1. Introduction*. Introduces async. Design and potential benefits and applications. **Highlight Paper**: "Loihi: A Neuromorphic Manycore Processor with On-Chip Learning," M. Davies et. al., *IEEE Micro*, 2018.	Intro to Verilog	HW #1: Verilog
2 **1/17**	Asynchronous Channels	**Required**: *Chapter 2. Channel-Based Design*. In depth analysis of various asynchronous channels.	SystemVerilog and SystemVerilogCS P	HW#2: SystemVerilogCSP
3 **1/24**	Modeling Asynchronous Circuits; Slack and Deadlock	**Required**: *Chapter 3. Modeling channel-based design.* Modeling of asynchronous designs using Verilog CSP.		
4 **1/31**	Pipeline performance Data-limited Bubble-limited Triangle Graphs	**Required**: *Chapter 4. Pipeline performance* Performance of asynchronous pipelines.	HW#3	HW #3: Linear pipelines and rings.
5 **2/7**	Design Styles Overview / Logic Hazards	**Required.** *Chapter 7. Taxonomy of asynchronous design styles. Chapter. Controller Design* *s*		
6 **2/14**	Network on Chips Fundamentals Metastability, Asynchronous Arbitration, Router Design, NoCs	**Required**. "Multiprocessor System-on-Chip, Chapter 1, An Introduction to Multi-Core System on Chip – Trends and Challenges", Springer, 2011	Review for Midterm	
7 **2/21**	Introduction to Class Project / ML Acceleration	**Required:** Y. Chen et al., "Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks," in *IEEE JSCC*, 2017.	Project presentation & report prep	Class Project Team Plan Due
8 **2/28**	Deeper Dive - Accelerating Spiking Neural Networks Midterm (tentative)	**Midterm Review**		
9 **3/7**	Bundled Data Design and BD Controllers (BM/Click)	**Required**: *Chapter 9: Micropipelines.* **Supplemental:** "Micropipelines" I. E. Sutherland, *Comm. of the ACM*, Vol 32 Issue 6, June 1989.	Edge / Minimalist	HW#4: Micropipelines / Minimalist / Click
3/14	Spring Break			

10 **3/21**	Quasi-Delay Insensitive (QDI) Pipelines Completion Sensing Proteus Flow	**Required**: *Chapter 11. QDI Templates.* **Highlight Paper:** Beerel, Peter A. et al. "Proteus: An ASIC Flow for GHz Asynchronous Designs." *IEEE Design & Test of Computers* 28 (2011): 36-51.	HW#5	HW#5:QDI design / Proteus HW
11 **3/28**	Timing Resilient and Radiation Hardened Design and Asynchronous Circuits	***Guest Lecture: Georgios Dimou, Niobium Systems (tentative)*** **Supplemental:** "SafeRazor: Metastability-Robust Adaptive Clocking in Resilient Circuits," M. Cannizzaro, et. al., IEEE TCAS I, Sept. 2015. **Highlight Paper:** "SERAD: Soft Error Resilient Asynchronous Design Using a Bundled Data Protocol," S. Aketi et. al, IEEE TCAS, May, 2020.	Project presentation & report prep	
12 **4/4**	Advanced performance analysis: Marked graphs, cycle times, Karp's Theorem, LP formulation, slack matching	**Required**: Chapter 5. Performance analysis. Mathematical approaches to model and optimize performance of asynchronous designs.	HW#8 Performance optimization	
13 **4/11**	Synchronizers & Metastability Containing Circuits, GALS	**Highlight Paper**: "Metastability and Synchronizers: A Tutorial", R. Ginosar, *IEEE Design & Test*, Sept/Oct. 2011. **Highlight Paper:**: "A Fine-Grained GALS SoC with Pausible Adaptive Clocking in 16 nm FinFET", M. Fojtik et al., *ASYNC* 2019.	Project Checkin	HW#8: Performance optimization
14 **4/18**	Buffer & Class Project Presentations			
15 **4/25**	Class Project Presentations		Final Exam Review	Class Project Final Report
FINAL	Date: Consult Schedule of Classes at classes.usc.edu/.			

Statement on Academic Conduct and Support Systems

Academic Conduct:

Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in SCampus in Part B, Section 11, "Behavior Violating University Standards" policy.usc.edu/scampus-part-b. Other forms of academic dishonesty are equally unacceptable. See additional information in SCampus and university policies on scientific misconduct, policy.usc.edu/scientific-misconduct.

Support Systems:

Student Health Counseling Services - (213) 740-7711 – 24/7 on call
engemannshc.usc.edu/counseling
Free and confidential mental health treatment for students, including short-term psychotherapy, group counseling, stress fitness workshops, and crisis intervention.

National Suicide Prevention Lifeline - 1 (800) 273-8255 – 24/7 on call
suicidepreventionlifeline.org
Free and confidential emotional support to people in suicidal crisis or emotional distress 24 hours a day, 7 days a week.

Relationship and Sexual Violence Prevention Services (RSVP) - (213) 740-4900 – 24/7 on call
engemannshc.usc.edu/rsvp
Free and confidential therapy services, workshops, and training for situations related to gender-based harm.

Office of Equity and Diversity (OED) | Title IX - (213) 740-5086
equity.usc.edu, titleix.usc.edu
Information about how to get help or help a survivor of harassment or discrimination, rights of protected classes, reporting options, and additional resources for students, faculty, staff, visitors, and applicants. The university prohibits discrimination or harassment based on the following protected characteristics: race, color, national origin, ancestry, religion, sex, gender, gender identity, gender expression, sexual orientation, age, physical disability, medical condition, mental disability, marital status, pregnancy, veteran status, genetic information, and any other characteristic which may be specified in applicable laws and governmental regulations.

Bias Assessment Response and Support - (213) 740-2421
studentaffairs.usc.edu/bias-assessment-response-support
Avenue to report incidents of bias, hate crimes, and microaggressions for appropriate investigation and response.

The Office of Disability Services and Programs - (213) 740-0776
dsp.usc.edu
Support and accommodations for students with disabilities. Services include assistance in providing readers/notetakers/interpreters, special accommodations for test taking needs, assistance with architectural barriers, assistive technology, and support for individual needs.

USC Support and Advocacy - (213) 821-4710
studentaffairs.usc.edu/ssa
Assists students and families in resolving complex personal, financial, and academic issues adversely affecting their success as a student.

Diversity at USC - (213) 740-2101
diversity.usc.edu
Information on events, programs and training, the Provost's Diversity and Inclusion Council, Diversity Liaisons for each academic school, chronology, participation, and various resources for students.

USC Emergency - UPC: (213) 740-4321, HSC: (323) 442-1000 – 24/7 on call
dps.usc.edu, emergency.usc.edu
Emergency assistance and avenue to report a crime. Latest updates regarding safety, including ways in which instruction will be continued if an officially declared emergency makes travel to campus infeasible.

USC Department of Public Safety - UPC: (213) 740-6000, HSC: (323) 442-120 – 24/7 on call
dps.usc.edu
Non-emergency assistance or information.