EE354L: Introduction to Digital Circuits

Course Number & Title: **EE354L: Introduction to Digital Circuits**

Units: 4

Semester and time: Fall 2022 semester
https://classes.usc.edu/term-20223/course/ee-354/
Lecture: MW 10:00-11:50 AM in GFS207 (also on Zoom)
Labs: 2 labs each lab 2H 50M in OHE336
(i) 5:00-7:50 PM Wed. (ii) 5:00-7:50 PM Thurs.

Location: Lectures: in person in GFS207; Labs in person in OHE336

Instructor: Gandhi Puvvada

Office: EEB 238 (But office hours are observed in EEB 203)

Office hours: 4 hours 4:10-6:00PM MW in EEB203
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/Gandhi_Office_Hours/Gandhi_Office_Hours_Fall2022.pdf

Contact information: gandhi@usc.edu, ~~Office: (213) 740-4461~~, Cell: (310) 733-8025

Catalog Description:

https://catalogue.usc.edu/

EE 354L Introduction to Digital Circuits (4, FaSpSm)
Digital system design and implementation; synchronous design of datapath and control; schematic/Verilog-based design, simulation, and implementation in Field Programmable Gate Arrays; timing analysis; semester-end project. *Prerequisite:* EE 109L

Learning objectives:

Upon completion of this course students will be able to:
1. Design, simulate, and build (implement on a FPGA board) a substantial digital system
2. Design a digital system using Verilog HDL (Hardware Description Language)
3. Understand RTL design (DPU and CU) and Timing design
4. Understand the use of an embedded processor in a digital system design
5. Compare dedicated hardware implementation with a processor-based implementation
6. Understand an 8-bit processor pinout, address decoding and SRAM memory interface
7. Understand issues with Clock domain crossing, 4-way and 2-way handshake, single-clock and two-clock FIFOs (First-In First-Out buffers) and their application
8. Understand tristate buffers, open-drain devices, buses, bus arbiters, rotating prioritizer
9. Understand how serial busses work, and get to know I2C bus operational details
10. Finally design and implement a semester-end project

Website: https://blackboard.usc.edu/

TAs: EE354L Wed Lab TA -- Sasindu Kangara Mudiyanselage <kangaram@usc.edu>
EE354L Thurs Lab TA – TBA

Course Mentors:
The 2 TAs are also Mentors for the lab part of the course.
Mentor cum Grader: EE354L Mentor-cum-Grader -- TBA 2 hours per week (TBA)
Will help you mainly on lecture material and homeworks.

Office hours: 1. Gandhi 4:10-6:00PM MW
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/Gandhi_Office_Hours/Gandhi_Office_Hours_Fall2022.pdf
2. All EE354L Hours: EE354L_Office_Hours_Fall2022.pdf (to be created for Fall 2022)

Prerequisite: EE109L (Introduction to Embedded Systems) Please review the later half of EE109L dealing with sequential logic, state machines, processor organization (design of a CPU), and FPGAs.
Recommended Preparation: Logic design and programming skills taught in courses like EE109L. Please review
EE109Unit14_HWStateMachines.pdf,
EE109Unit15_HWComponents.pdf,
EE109Unit16_ProcessorOrg.pdf,
EE109Unit18_MemoryFPGAs.pdf
EE109_State_Machine_CLB_review.mp4 ,
EE109_Fa20_Sp21_Finals_state_machine_and_CLB_review.pdf ,
EE109_Adders_Datapath_review.mp4 ,
EE109_Fa20_Sp21_Finals_adders_and_datapath.pdf.
Optional Textbook: Digital Design: Principles and Practices, 4/E By John F. Wakerly
http://www.ddpp.com/
Required class-notes and lab manual: Class-notes and Lab Manual

Recommended Reading: The lecture-by-lecture topic list in the last few pages of this syllabus is tentative and may change. Lecture sequence needs to adapt to the lab sequence. We will maintain a list of lecture topics "taught/to be taught" and convey (through an email) what we are going to cover in the next lecture. Please browse through the pdf files associated with the lecture for 10 minutes so that you are generally aware of the topic and slide sets. After each lecture, please spend at least 20 minutes that night (before you forget) browsing through the covered slides and note down points needing clarification. Discuss those points during our office hours. And, on weekend, please spend an hour or two to completely learn the material of that week's lectures and lab.

Course Material: Class-notes and Lab Manual

EE354L is an intensive design course, reinforcing class-room lectures with homework and lab assignments.
Textbooks often fail to cover the design process adequately. The lecture material and the lab assignments were developed over the last 30+ years of teaching this subject. It may look slightly unorganized, but it has all the material. I keep several past exams open. So, you have abundant practice material available to make use of.

Attendance policy: https://viterbi-web.usc.edu/www-classes/engr/ee-s/254/ee354l_attendance.html

Grading Policy (approximate weights) (approximately 45% in assignments and 55% in exams)**:**
Weights vary slightly from semester to semester. Example: Fall 2021 Grade sheet
Also, we use two scales (weights) for the three exams to compute the exam total and take the higher of the two for each student, so that if one does poorly in the Quiz+Midterm, he/she can try to do better in the final.

	Weight 1	Weight 2
HW	5.25	5.25
Short Exercises	2.75	2.75
LAB	24.00	24.00
Project	10.00	10.00
TA	3.00	3.00
Quiz	9.50	10.50
MT	20.50	24.50
Final	25.00	20.00
	100.00	100.00

Class Tentative Schedule: The order of lectures/topics changes a lot each semester.
Listed below are tentative dates for the lectures and labs. We will separately maintain a list of topics "taught/to be taught" in **ee354L topics covered in Fall2022.docx** and **revise it every week progressively**.

We have two lab sessions every week: 5-7:50 PM Wednesday & Thursday in OHE336. Wed. Thur. Stands for Wed. and Thurs.

Lec/Lab	Date	Day	Topics and Assignments
	August		
Lec#1	22	Mon	Course intro., Syllabus pdf , Logistics pdf , Office Hours pdf Topics covered .docx Nexys-4 (FPGA Board) Intro. Time-Division multiplexed 7-segment Common Anode Display Nexys4_Basic_IO_Introduction.pdf Nexys_4_documentation/ Vivado_installation/ (Old Nexys 3 pdf pdf .avi)
Lec#2	24	Wed	DPU & CU (Data Path Unit and Control Unit), One-hot state assignment for CU design pdf .wmv , ME (Mutually Exclusive) and AI (All Inclusive) rules in designing a state diagram pdf .avi ; State diagram Design examples .pdf .avi Detour lab pdf HW#5 Example of One-hot state assignment for CU design pdf dir
Lab#1		Wed. Thur.	Nexys-3/Nexys-4 (FPGA Board) Intro. Time-Division multiplexed 7-segment Common Anode Display pdf pdf .avi Detour Signal State Machine (Schematic) pdf .avi (Vivado 2019.2 for Synthesis, Modelsim for Simulation, etc.)
Lec#3	29	Mon	Data registers -- clocking and controlling pdf .avi ; Mealy machine example -- Divider Design pdf .avi ,
Lec#4	31	Wed	Introduction to the number lock lab. Verilog HDL Introduction pdf .avi , 0_Verilog_Main_Points_of_the_6_Lectures.pdf Verilog introduction, event driven simulation, cycle driven simulation, delta-T associated with non-blocking assignments which is crucial for successful simulation of a zero-delay modeling of a sequential logic (having Flip-Flops) (example: shift register)

	September		
Lab#2		Wed. Thur.	Detour Signal State Machine (Schematic) pdf .avi
	5	Mon	Labor Day, university holiday calendar
Lec#5	7	Wed	Sync_Counter_with_clr_load_en.pdf to illustrate Intercept and Inject method of building data path. .avi To make HDL coding readable and maintainable, there is an important need to reduce number of concurrent items by combining related logic together (example: deep combinational logic, where blocking assignments are important). Verilog Blocking and Non-blocking assignments, RTL coding in Verilog .pdf .avi .zip
Lab#3		Wed. Thur.	Verilog Introduction Labs (Synchronous and Asynchronous FF resets, and Divider RTL design in Verilog example design, Divider Moore machine design) .pdf .pdf .avi .pdf .zip
Lec#6	12	Mon	Loop Counter Incrementation and Terminal Value Checking pdf .avi pdf pdf pdf Verilog HDL behavioral modeling pdf .avi Verilog HDL Data types pdf .avi and Sequential Statements pdf .avi
Lec#7	14	Wed	Lab #6a RTL Coding -- Divider Example -- Debouncing, Single-stepping, and output coding pdf & .avi
Lab#4		Wed. Thur.	Number Lock State Machine, Nexys-4 Top design, all in Verilog .dir pdf
Lec#8	19	Mon	State machine design examples
Lec#9	21	Wed	**Picoblaze** The following is a quick introduction to the topics below as a prelude to introducing PicoBlaze in the next lecture. Introduction to Memories, Processors, Processor pinout, Processor Address Map, Byte Addressability, Processor address decoding, I/O addresses, I/O ports, Input port may or may not require a storage register to hold input data before collection by the processor, Output port needs a storage register to hold the output data sent by the processor for display or transmission, Interrupts, Interrupt service routine, sharing a single interrupt request (INTR) pin and identifying the requester. PicoBlaze is not for data crunching, it is meant to provide control sequences to perform a job such as UART, etc.
Lab#5		Wed. Thur.	Lab #6a RTL Coding -- Divider Example -- Debouncing, Single-stepping, and output coding pdf & .avi
Lec#10	26	Mon	Picoblaze introduction, Picoblaze Assembly Language, dir pdf pdf pdf 1.mp4 2.mp4
Lec#11	28	Wed	Data-path design (a) small system design .pdf .avi BCD to Binary and reverse conversion Chapter 7 , Inches to Yards-Feet-Inches conversion pdf .avi, GCD design pdf .avi
Lab#6		Wed. Thur.	GCD (Greatest Common Divisor) design .pdf
	October		
Lec#13	3	Mon	**Quiz (~10%): Monday, Oct. 3, 2022, 10:00-11:50 AM in _____**
Lec#14	5	Wed	Slack (make up)
Lab#7		Wed. Thur.	Picoblaze introduction, EE354L_Get_acquainted_with_PicoBlaze.pdf .pdf

Lec#15	10	Mon	Array processing in RTL, pointers and pointer incrementation, HW#8A .pdf Due dates and info: .pdf Directory .dir
Lec#16	12	Wed	Picoblaze interface to external hardware, input and output ports, ~~Hex Keypad .pdf .pdf .pdf~~ Picoblaze Interrupts .pdf (covered through a pre-recorded 8-part lecture mp4.zip posted at dir)
Lab#8		Wed. Thur.	Writing Testbenches .dir .pdf Fall Recess Oct 14-15 Calendar
Lec#17	17	Mon	Timing Design part 1 setup and hold margins, synchronizing asynchronous inputs .pdf HW#8 on Data Path Unit Design .pdf sol.pdf (~~.pdf .wmv.zip~~)
Lec#18	19	Wed	Timing Design part 2 reset synchronization, Shannon's expansion theorem applications .pdf Midterm review: Q#5 from Fall 2019 MT pdf sol.pdf Q#5 from Sp2020 MT .pdf sol.pdf Q#5 from Sp2020 Final .pdf sol.pdf
Lab#9		Wed. Thur.	Divider_Pico_N4 pdf dir ~~Keypad interface to Picoblaze .pdf~~ , ~~Demo: Divider on Pico .zip~~
Lec#19	24	Mon	Tristate Buffers, muxes and tristate buffers, HW#8 on Datapath ee101_hw_on_datapath.pdf sol.pdf
Lec#20	26	Wed	Decade counter pdf .zip Verilog HDL Blocking and Non-blocking assignments Last two pages pdf pdf .avi Verilog Exam questions review .pdf P1.avi P2.avi
Lab #10		Wed. Thur.	Picoblaze Interrupts (i) using polling (ii) with no polling Readme dir .pdf
Lec#21	31	Mon	**MT (~22.5%): *Monday, Oct. 31, 2022, 09:00 AM to 11:50 AM or 10:00 AM to 12:50 PM PST in _____*** Two choices, but let us try to find if one choice works for all 😊
	November		
Lec#22	2	Wed	Chapter 11 Memories .pdf .wmv
Lab #11		Wed. Thur.	Timing Analysis and Timing Constraints .pdf Prepare for the semester end project: PMODs, VGA demo, LCD demo, File I/O demo, Logic Analyzer Demo, ChipScope Demo, Final Project proposals
Lec#23	7	Mon	Memories lecture completion and FIFO lecture introduction, FIFOs .pdf .wmv
Lec#24	9	Wed	FIFO completion, Gray code, Binary<->Gray conversion, .pdf , Handshake .pdf .pdf
Lab #11		Wed. Thur.	Timing Analysis and Timing Constraints .pdf Prepare for the semester end project: PMODs, VGA demo, LCD demo, File I/O demo, Logic Analyzer Demo, ChipScope Demo, Final Project proposals
Lec#25	14	Mon	Ch 4_mux, Barrel shifters, priority encoders, Totem-pole and Open-collector output devices dir New.pdf OLD.pdf .mp4
Lec#26	16	Wed	Make-up lecture
Lab #12		Wed. Thur.	Final Project proposals approvals, Final Project Week 1
Lec#27	21	Mon	UART Basics .pdf , I2C Bus Protocol .pdf .mp4 exam_Q.pdf
~~Lec#28~~	23	~~Wed~~	Thanksgiving Break Nov 23-27 calendar
~~**Lab #13**~~		~~Wed. Thur.~~	Final Project Week 2 (at home due to Thanksgiving break)
Lec#29	28	Mon	Chapter #10 Selected parts of the counter topic -- basics of Ripple and Synchronous counters .pdf Special Counters Exam questions .pdf .pdf .pdf
	December		

Lec#30	30	Wed	Review for the Final exam (bubble to bubble logic from .pdf)
Lab #14		Wed. Thur.	Final Project demonstration, presentation, and report submission
	Dec. 3-6	Sat-Tues	Study days calendar
	12	Monday	Official Final Exam time is as given below. But I am requesting the class to agree to the change proposed further below. ========== https://classes.usc.edu/term-20223/finals/ 10 or 10:30 MWF Monday, December 12 8-10 a.m.
	12	Monday	**Final (~22.5%): Monday, Dec. 12, 2022, 07:30-10:30 AM (official exam slot 08:00-10:00 AM)** Sorry 7:30 AM is too early, but … Please help me and the class by agreeing to the 3-Hour exam time. We start the exam 30 min. early and end the exam 30 min. late . Thanks! I have checked the finals schedule and found that there is no conflict with the proposed extended time.

Continued on the next page

Statement on Academic Conduct and Support Systems

Academic Conduct:

Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in SCampus in Part B, Section 11, "Behavior Violating University Standards" policy.usc.edu/scampus-part-b. Other forms of academic dishonesty are equally unacceptable. See additional information in SCampus and university policies on scientific misconduct, policy.usc.edu/scientific-misconduct.

Support Systems:

Counseling and Mental Health - (213) 740-9355 – 24/7 on call

studenthealth.usc.edu/counseling

Free and confidential mental health treatment for students, including short-term psychotherapy, group counseling, stress fitness workshops, and crisis intervention.

National Suicide Prevention Lifeline - 1 (800) 273-8255 – 24/7 on call

suicidepreventionlifeline.org

Free and confidential emotional support to people in suicidal crisis or emotional distress 24 hours a day, 7 days a week.

Relationship and Sexual Violence Prevention Services (RSVP) - (213) 740-9355(WELL), press "0" after hours – 24/7 on call

studenthealth.usc.edu/sexual-assault
Free and confidential therapy services, workshops, and training for situations related to gender-based harm.

Office of Equity and Diversity (OED) - (213) 740-5086 | Title IX – (213) 821-8298

equity.usc.edu, titleix.usc.edu
Information about how to get help or help someone affected by harassment or discrimination, rights of protected classes, reporting options, and additional resources for students, faculty, staff, visitors, and applicants.

Reporting Incidents of Bias or Harassment - (213) 740-5086 or (213) 821-8298

usc-advocate.symplicity.com/care_report

Avenue to report incidents of bias, hate crimes, and microaggressions to the Office of Equity and Diversity |Title IX for appropriate investigation, supportive measures, and response.

Office of Student Accessibility Services (OSAS)(previously called Disability Services and Programs(DSP))- (213) 740-0776

https://osas.usc.edu

Support and accommodations for students with disabilities. Services include assistance in providing readers/notetakers/interpreters, special accommodations for test taking needs, assistance with architectural barriers, assistive technology, and support for individual needs.

USC Campus Support and Intervention - (213) 821-4710
campussupport.usc.edu

Assists students and families in resolving complex personal, financial, and academic issues adversely affecting their success as a student.

Diversity at USC - (213) 740-2101

diversity.usc.edu

Information on events, programs and training, the Provost's Diversity and Inclusion Council, Diversity Liaisons for each academic school, chronology, participation, and various resources for students.

USC Emergency - UPC: (213) 740-4321, HSC: (323) 442-1000 – 24/7 on call

dps.usc.edu, emergency.usc.edu

Emergency assistance and avenue to report a crime. Latest updates regarding safety, including ways in which instruction will be continued if an officially declared emergency makes travel to campus infeasible.

USC Department of Public Safety - UPC: (213) 740-6000, HSC: (323) 442-120 – 24/7 on call dps.usc.edu

Non-emergency assistance or information.