EE354L: Introduction to Digital Circuits

Course Number & Title: **EE354L: Introduction to Digital Circuits**

Units: 4

Semester and time: Spring 2022 semester
https://classes.usc.edu/term-20221/course/ee-354/
Lecture: MW 10:00-11:50 AM in RTH105
Labs: 3 labs each lab 2H 50M in OHE336
(i) 5:00-7:50 PM Tues. (iii) 4:30-7:20 PM Wed. (iv) 6:00-8:50 PM Thurs.
Friday 5-8:50 PM Quiz (this Quiz slot is used only 2 times in the semester)

Location: Lectures: RTH105; Labs in OHE336

Instructor: Gandhi Puvvada

Office: EEB 238 (but office hours are observed in EEB203)

Office hours: 4 hours per week
4:10-5:30PM MW in EEB 203/Zoom and 9:00-10:00 AM on Tuesday on Zoom
http://www-classes.usc.edu/engr/ee-s/457/Gandhi_Office_Hours/Gandhi_Office_Hours_Sp2022.pdf

Contact information: gandhi@usc.edu, ~~Office: (213) 740-4461~~, Cell: (310) 733-8025 (Try to email me)

Catalog Description:

https://catalogue.usc.edu/

EE 354L Introduction to Digital Circuits (4, FaSpSm)
Digital system design and implementation; synchronous design of datapath and control; schematic/Verilog-based design, simulation, and implementation in Field Programmable Gate Arrays; timing analysis; semester-end project. *Prerequisite:* EE 109L. (Duplicates credit in EE 254.)

Learning objectives:

Upon completion of this course students will be able to:
1. Design, simulate, and build (i.e., implement on a FPGA board) a substantial digital system
2. Design a digital system using Verilog HDL (Hardware Description Language)
3. Understand RTL design (DPU and CU) and Timing design
4. Understand the use of an embedded processor in a digital system design
5. Compare dedicated hardware implementation with a processor-based implementation
6. Understand 8-bit processor pinout, address decoding and SRAM memory interface
7. Understand issues with Clock domain crossing, 4-way and 2-way handshake, single-clock and two-clock FIFOs (First-In First-Out buffers) and their application
8. Understand tristate buffers, open-drain devices, buses, bus arbiters,
9. Understand rotating prioritizers and how to build them using barrel shifters
10. Understand how serial busses work, and get to know I2C bus operational details
11. Finally design and implement a semester-end project

Website: https://blackboard.usc.edu/

TAs:
EE354L Tues Lab TA -- Sasindu Kangara Mudiyanselage kangaram@usc.edu
EE354L Wed Lab TA -- Jing lei Cheng chen520@usc.edu
EE354L Thurs Lab TA -- Chao Wang wang484@usc.edu

Course Mentors:
Besides the 3 TAs we expect to have two Mentors for this course (one for the lab and one for the lecture/homework material). The lab mentor will be available for 1.5 hours in each of the three labs. The lecture/homework mentor will hold 4.5 hours of office hours per week.

Grader: The lecture/homework mentor is also a grader for this course.
EE354L Mentor-cum-Grader -- Piyush Pandey <piyushp@usc.edu>

Office hours: 1. Gandhi_Office_Hours_Sp2022.pdf 4:10-5:30 PM MW in EEB203/Zoom;
9:00-10:00 AM Tuesday on Zoom
2. TAs' Hours: TBA

3. Mentor-cum-Grader Hours: TBA

Prerequisite: EE109L https://bytes.usc.edu/ee109/schedule/
Please go through the following 4 lecture slides and two webcasts
EE109Unit14_HWStateMachines.pdf, EE109Unit15_HWComponents.pdf, EE109Unit16_ProcessorOrg.pdf, EE109Unit18_MemoryFPGAs.pdf
EE109_State_Machine_CLB_review.mp4 , .EE109_Fa20_Sp21_Finals_state_machine_and_CLB_review.pdf ,
EE109_Adders_Datapath_review.mp4 , EE109_Fa20_Sp21_Finals_adders_and_datapath.pdf

Recommended Preparation: Basic programming skills taught in courses like EE109L (Introduction to Embedded Systems)

Optional Textbook: Digital Design: Principles and Practices, 4/E By John F. Wakerly http://www.ddpp.com/

Required class-notes and lab manual: Class-notes and Lab Manual distributed online progressively

Recommended Reading: The lecture-by-lecture topic list in the last few pages of this syllabus is tentative and may change substantially as we are revising the labs and lecture sequence this semester. Sometimes the lecture sequence may abruptly change its order abruptly so as to adopt to the lab sequence. But we will convey (through an email) at least a day before the lecture what we are going to cover in that lecture. Please browse through the pdf files associated with the lecture for 10 minutes so that you are generally aware of the topic and slide sets. After each lecture, that night (before you forget), please spend at least 20 minutes to browse through the covered slides to note down points needing clarification and discuss them during our office hours. And on weekend, spend an hour or two to completely learn the material of that week's lectures.

Course Material: Class-notes and Lab Manual

EE354L is an intensive design course, reinforcing class-room lectures with homework and lab assignments. Textbooks often fail to cover the design process adequately. The lecture material and the lab assignments were developed over the last 30 years of teaching this subject. It may look slightly unorganized, but it has all the material. I keep all the past exams open. So, you have abundant practice material available to make use of.

Attendance policy: http://www-classes.usc.edu/engr/ee-s/254/ee354l_attendance.html

Grading Policy (approximate weights) (approximately 45% in assignments and 55% in exams)**:**
Weights vary slightly from semester to semester. Example: Fall 2021 Grade sheet
Also, we use two scales (weights) for the three exams to compute the exam total and take the higher of the two for each student, so that if some students do poorly in their Quiz and Midterm, they can try to do better in their final (or if a few students have a bad luck in their final, their Quiz and MT scores would weight more in their overall letter grade).

	Weight 1	Weight 2
HW	5.25	5.25
Short Exercises	2.75	2.75
LAB	24.00	24.00
Project	10.00	10.00
TA	3.00	3.00
Quiz	10.00	11.00
MT	20.50	23.50
Final	24.50	20.50
	100.00	100.00

Class Tentative Schedule: Topics and the order of lectures change a lot this semester as we are hoping to revise the course content.
Listed below are the dates for the lecture and the lab and the past semester. We will revise this list progressively. https://classes.usc.edu/term-20221/course/ee-354/

TWT (in the lab rows below) stands for Tuesday, Wednesday, and the Thursday and refers to the four labs every week.

Lec/Lab	Date	Day	Topics and Assignments
	January		
Lec#1	10	Mon	Course intro., Nexys-4 (FPGA Board) Intro. Time-Division multiplexed 7-segment Common Anode Display Nexys4_Basic_IO_Introduction.pdf Nexys_4_documentation/ Vivado_installation/ (Old Nexys 3 pdf pdf .avi)
Lec#2	12	Wed	DPU & CU (Data Path Unit and Control Unit), One-hot state assignment for CU design pdf .wmv , ME (Mutually Exclusive) and AI (All Inclusive) rules in designing a state diagram pdf .avi ; State diagram Design examples .pdf .avi Detour lab pdf HW#5 Example of One-hot state assignment for CU design pdf dir
Lab#1		TWT	Lab introduction pdf, Tools installation pdf (Vivado for Synthesis, Modelsim for Simulation, etc.) , VDI, distribute Nexys 4 boards and test them using test_nexys4_verilog.zip
Lec#3	17	Mon	Martin Luther King Day, university holiday calendar

Lec#4	19	Wed	Data registers -- clocking and controlling pdf .avi ; Mealy machine example -- Divider Design pdf .avi ,
Lab#2		TWT	Nexys-4 (FPGA Board) Intro. Time-Division multiplexed 7-segment Common Anode Display pdf pdf .avi Detour Signal State Machine (Schematic) detour.pdf (Old Nexys 3 detour pdf .avi)
Lec#5	24	Mon	Introduction to the number lock lab. Verilog HDL Introduction pdf .avi , 0_Verilog_Main_Points_of_the_6_Lectures.pdf Verilog introduction, event driven simulation, cycle driven simulation, delta-T associated with non-blocking assignments which is crucial for successful simulation of a zero-delay modeling of a sequential logic (having Flip-Flops) (example: shift register)
Lec#6	26	Wed	Sync_Counter_with_clr_load_en.pdf to illustrate Intercept and Inject method of building data path. .avi To make HDL coding readable and maintainable, there is an important need to reduce number of concurrent items by combining related logic together (example: deep combinational logic, where blocking assignments are important). Verilog Blocking and Non-blocking assignments, RTL coding in Verilog .pdf .avi .zip
Lab#3		TWT	Number Lock State Machine paper design of core and the top, Detour Verilog core design simulation in Modelsim.
Lec#7	31	Mon	Loop Counter Incrementation and Terminal Value Checking pdf .avi pdf pdf pdf Verilog HDL behavioral modeling pdf .avi Verilog HDL Data types pdf .avi and Sequential Statements pdf .avi
	February		
Lec#8	2	Wed	Lab #6a RTL Coding -- Divider Example -- Debouncing, Single-stepping, and output coding pdf & .avi
Lab#4		TWT	Verilog Introduction Labs (Synchronous and Asynchronous FF resets, and Divider RTL design in Verilog example design, Divider Moore machine design) .pdf .pdf .avi .pdf .zip Number Lock State Machine, Nexys-4 Top design, all in Verilog .dir pdf
Lec#9	7	Mon	State machine design examples
Lec#10	9	Wed	**Picoblaze** The following is a quick introduction to the topics below as a prelude to introducing PicoBlaze in the next lecture. Introduction to Memories, Processors, Processor pinout, Processor Address Map, Byte Addressability, Processor address decoding, I/O addresses, I/O ports, Input port may or may not require a storage register to hold input data before collection by the processor, Output port needs a storage register to hold the output data sent by the processor for display or transmission, Interrupts, Interrupt service routine, sharing a single interrupt request (INTR) pin and identifying the requester. PicoBlaze is not for data crunching, it is meant to provide control sequences to perform a job such as UART, etc.
Lab#5		TWT	Lab #6a RTL Coding -- Divider Example -- Debouncing, Single-stepping, and output coding pdf & .avi
Lec#11	14	Mon	Picoblaze introduction, Picoblaze Assembly Language, dir pdf pdf pdf 1.mp4 2.mp4
Lec#12	16	Wed	Data-path design (a) small system design .pdf .avi BCD to Binary and reverse conversion Chapter 7 , Inches to Yards-Feet-Inches conversion pdf .avi, GCD design pdf .avi
Lab#6		TWT	GCD (Greatest Common Divisor) design .pdf
Lec#13	21	Mon	Presidents' Day, university holiday calendar
Lec#14	23	Wed	Quiz preparation
Lab#7		TWT	Picoblaze introduction, EE354L_Get_acquainted_with_PicoBlaze.pdf .pdf
	25	Fri	**Quiz Exam: 5:00PM-8:00 PM**
Lec#15	28	Mon	Array processing in RTL, pointers and pointer incrementation, HW#8A .pdf Due dates and info: .pdf Directory .dir

	March		
Lec#16	2	Wed	Picoblaze interface to external hardware, input and output ports, Hex Keypad .pdf .pdf .pdf Picoblaze Interrupts .pdf (covered through a pre-recorded 8-part lecture mp4.zip posted at dir)
Lab#8		TWT	Writing Testbenches .dir .pdf
Lec#17	7	Mon	Timing Design part 1 setup and hold margins, synchronizing asynchronous inputs .pdf HW#8 on Data Path Unit Design .pdf sol.pdf (~~.pdf~~ ~~.wmv.zip~~)
Lec#18	9	Wed	Timing Design part 2 reset synchronization, Shannon's expansion theorem applications .pdf Midterm review, Q#2, ~~Q#3~~ from Sp2013 .pdf sol.pdf [Note:Q#3 is truck off as it deals with a topic, "microprogrammed control unit", which is not being taught in recent years.]
Lab#9		TWT	Keypad interface to Picoblaze .pdf , Demo: Divider on Pico .zip
	14	Mon	March 13-20 Spring recess
	16	Wed	March 13-20 Spring recess
	18	TWT	March 13-20 Spring recess
Lec#19	21	Mon	Tristate Buffers, muxes and tristate buffers in Data-path design Q#2 MT_Sp12.pdf MT_Sp12_sol.pdf
Lec#20	23	Wed	Decade counter pdf .zip Verilog HDL Blocking and Non-blocking assignments Last two pages pdf pdf .avi Verilog Exam questions review .pdf P1.avi P2.avi
Lab #10		TWT	Picoblaze Interrupts (i) using polling (ii) with no polling Readme dir .pdf
Lec#21	28	Mon	Slack (make up), Midterm Review
Lec#22	30	Wed	Chapter 11 Memories .pdf .wmv
Lab #11		TWT	Timing Analysis and Timing Constraints .pdf Prepare for the semester end project: PMODs, VGA demo, LCD demo, File I/O demo, Logic Analyzer Demo, ChipScope Demo, Final Project proposals
	April		
	1	Fri	**Midterm Exam: 5:00PM-8:00 PM Thank you all for agreeing to this slot for a common exam**
Lec#23	4	Mon	
Lec#24	6	Wed	Memories lecture completion and FIFO lecture introduction, FIFOs .pdf .wmv
Lab #12		TWT	Final Project proposals approvals, Final Project Week 1
Lec#25	11	Mon	FIFO completion, Gray code, Binary<->Gray conversion, .pdf , Handshake .pdf .pdf
Lec#26	13	Wed	Ch 4_mux, Barrel shifters, priority encoders, Totem-pole and Open-collector output devices dir
Lab #13		TWT	Final Project Week 2
Lec#27	18	Mon	CLA (Carry Look-ahead Adder) dir
Lec#28	20	Wed	UART Basics .pdf , I2C Bus Protocol .pdf
Lab #14		TWT	Final Project Week 3

Lec#29	25	Mon	Chapter #10 Selected parts of the counter topic -- basics of Ripple and Synchronous counters .pdf Special Counters Exam questions .pdf .pdf .pdf Review for the Final exam (bubble to bubble logic from .pdf)
Lec#30	27	Wed	Review
Lab #15		TWT	Final Project demonstration, presentation, and report submission
	May		
	5	Thursday	**Final exam 7:30 AM – 10:30 AM** (All students, I request that you all please agree to this time extension) https://classes.usc.edu/term-20221/finals/ As per the **Exceptions** schedule at the bottom of the above page. Electrical Engineering 354 Thursday, May 5 8-10 a.m.

Continued on the next page

Statement on Academic Conduct and Support Systems

Academic Conduct:

Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in SCampus in Part B, Section 11, "Behavior Violating University Standards" policy.usc.edu/scampus-part-b. Other forms of academic dishonesty are equally unacceptable. See additional information in SCampus and university policies on scientific misconduct, policy.usc.edu/scientific-misconduct.

Support Systems:

Counseling and Mental Health - (213) 740-9355 – 24/7 on call

studenthealth.usc.edu/counseling

Free and confidential mental health treatment for students, including short-term psychotherapy, group counseling, stress fitness workshops, and crisis intervention.

National Suicide Prevention Lifeline - 1 (800) 273-8255 – 24/7 on call

suicidepreventionlifeline.org

Free and confidential emotional support to people in suicidal crisis or emotional distress 24 hours a day, 7 days a week.

Relationship and Sexual Violence Prevention Services (RSVP) - (213) 740-9355(WELL), press "0" after hours – 24/7 on call

studenthealth.usc.edu/sexual-assault

Free and confidential therapy services, workshops, and training for situations related to gender-based harm.

Office of Equity and Diversity (OED) - (213) 740-5086 | Title IX – (213) 821-8298

equity.usc.edu, titleix.usc.edu

Information about how to get help or help someone affected by harassment or discrimination, rights of protected classes, reporting options, and additional resources for students, faculty, staff, visitors, and applicants.

Reporting Incidents of Bias or Harassment - (213) 740-5086 or (213) 821-8298

usc-advocate.symplicity.com/care_report

Avenue to report incidents of bias, hate crimes, and microaggressions to the Office of Equity and Diversity |Title IX for appropriate investigation, supportive measures, and response.

The Office of Disability Services and Programs - (213) 740-0776

dsp.usc.edu

Support and accommodations for students with disabilities. Services include assistance in providing readers/notetakers/interpreters, special accommodations for test taking needs, assistance with architectural barriers, assistive technology, and support for individual needs.

USC Campus Support and Intervention - (213) 821-4710

campussupport.usc.edu

Assists students and families in resolving complex personal, financial, and academic issues adversely affecting their success as a student.

Diversity at USC - (213) 740-2101

diversity.usc.edu

Information on events, programs and training, the Provost's Diversity and Inclusion Council, Diversity Liaisons for each academic school, chronology, participation, and various resources for students.

USC Emergency - UPC: (213) 740-4321, HSC: (323) 442-1000 – 24/7 on call

dps.usc.edu, emergency.usc.edu

Emergency assistance and avenue to report a crime. Latest updates regarding safety, including ways in which instruction will be continued if an officially declared emergency makes travel to campus infeasible.

USC Department of Public Safety - UPC: (213) 740-6000, HSC: (323) 442-120 – 24/7 on call

dps.usc.edu

Non-emergency assistance or information.