IMPORTANT:
Please refer to the USC Center for Excellence in Teaching for current best practices in syllabus and course design. This document is intended to be a customizable template that primarily includes the technical elements required for the Curriculum Office to forward your proposal to the UCOC.

EE 477L MOS VLSI Circuit Design

Units: 4

Term—Day—Time: Fall 2021 TTh 2-3:20 PM

IMPORTANT:

Location: The permanent course website is at https://sites.google.com/usc.edu/ee477homepage/home , this semester's site is https://sites.google.com/usc.edu/ee477homepage/home/21-fall . The DEN link is at https://courses.uscden.net/d2l/home/21672

Instructor: Prof. Alice Parker

Office: parker@usc.edu

Office Hours: 2-3 PM MW

Contact Info: parker@usc.edu Timeline for replying to emails/calls (i.e. within 24 hours).

Teaching Assistant: TBD

Office: Physical or virtual address

Office Hours:

Contact Info: Email, phone number (office, cell), Skype, etc.

IT Help: Group to contact for technological services, if applicable.

Hours of Service:

Contact Info: Email, phone number (office, cell), Skype, etc.

Course Description

Course Objective: Learn fundamental techniques for the design of VLSI circuits, be able to design simple cells, and be able to configure chips containing the simple cells.

Course Outline: Analysis and design of digital MOS VLSI circuits including area, delay and power minimization. Laboratory assignments including design, layout, extraction, simulation and automatic synthesis.

Learning Objectives

The student completing EE 477L/ entering EE 577a should possess the following skills:

Logic Design:
Convert NAND circuits to NOR circuits and vice versa

Circuit Design - Combinational:
Provide transistor-level circuits for complementary CMOS NAND, NOR, and transmission gates, inverters, latches, and flip-flops.
Construct full-adder circuits to minimize area or maximize speed
Construct multiplexer circuits with transmission gates
Construct multiplexer circuits with complementary CMOS NAND and NOR gates
Construct compound complementary CMOS gates from Boolean equation specifications and vice versa
Construct a simple XOR gate

Circuit Design – Sequential:
Construct a circuit for a D flip flop that is positive/negative edge triggered, with asynchronous set/reset and a load signal
Construct asynchronously settable and resettable latches and flip flops

Circuit Design - Basic understanding of transistors:

Use unit-size and minimum size transistors in circuits
Identify source and drain of transistors in complementary CMOS circuits and transmission gates
Determine regions of operation of transistors in simple circuits, applying traditional inequalities
Explain the reasons for transmission of weak 1's in NMOS transistors and weak 0's in PMOS transistors
Detect transistors subject to the body effect and know the resultant changes in threshold voltage that occur.

Describe the physical changes that result when a positive voltage is applied to the gate of an enhancement-mode NMOS transistor, including accumulation, depletion and inversion
Locate parasitic MOS and bipolar transistors in simple CMOS layouts
Compute current I_{DS} in MOS transistors based on gate, source and drain voltages
State the relationship between MOS current and voltages, gate capacitance, transistor betas, carrier mobility, device sizes
Apply basic relationships between current flow, voltage and capacitance to analyze circuits
Compute effective channel resistance in the linear region, based on mobility, gate capacitance, channel length and channel width
Take into account channel length modulation when computing current flow in the saturation region
Determine the output voltage of a CMOS pass transistor given an input voltage and gate voltage over time
Determine regions of operation of pass transistors over time, given initial conditions

Circuit Design – Capacitance and equivalent circuits:
Compute worst-case gate capacitance using a parallel plate model
Approximate the gate capacitance in the cutoff, linear and saturation regions
Give an equivalent circuit for any MOS circuit, even with long wires
Compute diffusion capacitance given the relevant parameters
State the gross relationship between gate capacitance, diffusion capacitance, channel resistance, interconnect resistance and interconnect capacitance, and the rise/fall/delay for a CMOS circuit

Circuit Design - The Inverter:
Identify regions of operation of transistors in an inverter when the inverter is operating in different parts of the input/output transfer curve
Sketch the effect of the beta ratios of inverter transistors on the shape of the input/output transfer curve

Circuit Design – Delay computations:
Size transistors in complementary CMOS gates for equal worst case rise/fall times
Identify a critical path in a gate or logic circuit
Use lumped or distributed RC time constants to find critical paths in a logic diagram
Set limits on integration to compute rise/fall/delay for an inverter
Compensate for late and early clocks when designing flipflops
Identify the timing factors that contribute to clock cycle in a flip flop (setup, hold, clock to Q)
Compute lumped and distributed wire delays
Include inductance in an equivalent circuit for a wire
Determine whether L's must be included when modeling a particular situation
Compute Rint and Cint for wires
Estimate fringing field capacitance using a graph or equation
Estimate the RC time constant at any node in an equivalent circuit using Elmore delay even with fan out
Determine when to insert repeaters

Construct an inverter chain to drive a large capacitive load when diffusion capacitance is negligible and when it is not negligible.
Size devices in complementary CMOS circuits using the ratio method

Circuit design – Power Considerations:
Identify power consumption situations as static or dynamic
Know the relationship between oxide thickness and leakage power
State the relationship between switching frequency and power

Circuit design – Noise margins:
Compute noise margin for a CMOS circuit given V_{OH}, V_{OL}, V_{IH} and V_{IL}
Give definitions for V_{OH}, V_{OL}, V_{IH} and V_{IL} and understand how they can be obtained.

Circuit design – Dynamic circuits:

Design and analyze a dynamic latch and flip flop
Identify where charge sharing occurs and compute the effect on the circuit voltages
Construct dynamic and domino logic circuits
Adhere to rules about inputs changing in dynamic and domino logic circuits
Be able to produce timing diagrams for any MOS circuit, including dynamic and domino logic circuits
Construct 6 transistor and 1 transistor RAM circuits, and show timing diagrams for their operation

Physical Design:

Sketch stick diagrams of CMOS circuits using a typical cell design style
Sketch stick diagrams of compound CMOS gates using Euler paths to organize the physical design
Define the terms stacked contact, split contact, butting contact, and ohmic contact
Use a physical layout tool to design CMOS cells
Design a layout with multiple cells using simple area minimization strategies, including VDD and Gnd sharing, abutting connections, metal layer assignments and cell abutment in one or both directions
Use the left edge algorithm to connect common inputs/outputs in a routing channel

Fabrication:

Enumerate the steps in fabrication of typical CMOS chips in order
Enumerate the detailed steps in the photolithographic process
Understand the reasons for layout design rules
Show the 3D structure of a CMOS layout along a vertical cut through the substrate
Define the terms epitaxy, deposition, diffusion, and ion implantation

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Optional topics for EE 477L:

Subthreshold Current Conduction with equation
SR latch circuit including NAND and NOR implementations
Pipelined designs
Pipelined domino
NORA CMOS logic (NP domino logic)
DRAM array and bitline sensing
Leakage currents in DRAM cells
NOR and NAND ROM arrays, with row and column decoders

Prerequisite(s): Prerequisite: EE 327 or EE 338.

Co-Requisite(s): none
Concurrent Enrollment: none
Recommended Preparation: none

Textbook:

***CMOS Digital Integrated Circuits*, 4th edition, Kang, Leblebici and Kim, McGraw-Hill**

Other References:

***Integrated Circuits: A Design Perspective*, Jan Rabaey, Prentice Hall**

***Digital Integrated Circuit Design*, Martin, Oxford**

***CMOS VLSI Design: A Circuits and Systems Perspective*, Neil Weste and David Harris third edition, Addison Wesley**

Course Notes
Letter grading. Taught on DEN zoom. Copies of lecture slides and other class information will be posted on DEN.

Required Readings and Supplementary Materials
Required readings are shown in the course schedule. Materials not in the text will be posted on the DEN website.

Description and Assessment of Assignments
There will be 5 – 6 homework assignments, 2 laboratory assignments, and one final project.

Grading Breakdown

Including the above detailed assignments, how will students be graded overall? Participation should not exceed 15% of the total grade. Where it does, the syllabus must provide an added explanation. No portion of the grade may be awarded for class attendance but non-attendance can be the basis for lowering the grade, when clearly stated on the syllabus. The sum of percentages must total 100%.

Assessment Tool (assignments)	Points	% of Grade
Homework		10%
Labs/Final Project		40%
Midterms		50%
TOTAL		100%

Grading Scale

(Optional – the following is only an example of what one might look like if included)

Course final grades will be determined using the following scale

A	92-100
A-	90-91
B+	87-89
B	73-86
B-	70-72
C+	67-69
C	63-68
C-	60-62
D+	57-59
D	53-56
D-	50-52
F	49 and below

Assignment Submission Policy

Assignments are uploaded to DEN online at 5 PM on the due date. Late assignments will be penalized 5% for the first day and 10% each subsequent day up to 45% penalty.

Grading Timeline

2 weeks timeline for grading and feedback.

Additional Policies

Course Schedule: A Weekly Breakdown

Lecture #	Topics	Readings
Class Introduction **8/24**	Class Introduction	Chapter 1, 1.1-1.11, draft text pdf
2 8/26 **9/2**	Introduction to CMOS Circuits; MOS Transistor Theory, stick diagrams, transmission gates	Chapter 1, 1.1-1.11
3 8/31	Latches, CMOS Processing Technology and Fabrication	Chapter 2, 2.1-2.3
4 9/2	Fabrication	
5 **9/7**	CMOS Design Rules	Chapter 2, 2.4-2.5
6 **9/9**	MOS Transistor Theory - IV Characteristics	Chapter 3, 3.3 pp. 90-93,99-100, Sec. 3.4 through p. 106
7 **9/14**	MOS Transistor Theory - Capacitance, Threshold Voltage, Scaling	Chapter 3, 3.2, 3.3 pp. 94-98, 3.4, 3.5
8 9/16	Capacitance, Inverter Characteristics	Chapter 3, 3.6, Chapter 5, 5.4
9 **9/21**	Inverter Characteristics, Transmission Gate Characteristics	Chapter 5, 5.1, Chapter 6, 6.1
10 9/23	Fabrication Videos	
11 9/28	Midterm Review	
9/30	**Midterm Examination I - Tentative Date**	
12 10/5	Midterm Discussion	
13 10/7	Device Sizing	Course notes
14 10/12	CMOS Physical Design - Euler Paths	Chapter 7, Section 7.4
10/14	Fall break	
15 10/19	Interconnections, Layout Strategies	Course notes
16 10/21	Inverter Fall Time/Delay	Course notes, Chapter 6, 6.1-6.3
17 10/26	Inverter Delay	Chapter 6, 6.1-6.3
18 10/28	Delay and Inverter Optimization	Chapter 6, 6.1-6.4
19 11/2	Sequential Circuits and Interconnect Delay	Chapter 8, 8.1-8.2, 8.5, Chapter 6, 6.6

20 11/4	Interconnect Resistance and Capacitance, Interconnect Delay	Chapter 6, 6.5-6.6
21 11/9	Interconnection Delay	Course notes, Chap. 6, 6.4-6.6
22 11/11	Delay computations	Course notes
23 11/16	Super buffer design/ Ring Oscillators	Chapter 6 Appendix
24 11/18	Midterm review	
11/23	**Midterm Examination II - Tentative Date**	
11/25	Thanksgiving	
26 11/30	Midterm discussion	
27 12/1	Power consumption	Chap. 6, 6.7
Extra lecture	Dynamic circuits/Domino logic/Memories	Chapter 9
	Final project due	

There will not be a final exam. The final project will be due on the final exam date.

Statement on Academic Conduct and Support Systems

Academic Conduct:

Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in SCampus in Part B, Section 11, "Behavior Violating University Standards" policy.usc.edu/scampus-part-b. Other forms of academic dishonesty are equally unacceptable. See additional information in SCampus and university policies on scientific misconduct, policy.usc.edu/scientific-misconduct.

Support Systems:

Counseling and Mental Health - (213) 740-9355 – 24/7 on call
studenthealth.usc.edu/counseling
Free and confidential mental health treatment for students, including short-term psychotherapy, group counseling, stress fitness workshops, and crisis intervention.

National Suicide Prevention Lifeline - 1 (800) 273-8255 – 24/7 on call
suicidepreventionlifeline.org
Free and confidential emotional support to people in suicidal crisis or emotional distress 24 hours a day, 7 days a week.

Relationship and Sexual Violence Prevention Services (RSVP) - (213) 740-9355(WELL), press "0" after hours – 24/7 on call
studenthealth.usc.edu/sexual-assault
Free and confidential therapy services, workshops, and training for situations related to gender-based harm.

Office of Equity and Diversity (OED) - (213) 740-5086 | Title IX – (213) 821-8298
equity.usc.edu, titleix.usc.edu
Information about how to get help or help someone affected by harassment or discrimination, rights of protected classes, reporting options, and additional resources for students, faculty, staff, visitors, and applicants.

Reporting Incidents of Bias or Harassment - (213) 740-5086 or (213) 821-8298
usc-advocate.symplicity.com/care_report
Avenue to report incidents of bias, hate crimes, and microaggressions to the Office of Equity and Diversity |Title IX for appropriate investigation, supportive measures, and response.

The Office of Disability Services and Programs - (213) 740-0776
dsp.usc.edu
Support and accommodations for students with disabilities. Services include assistance in providing readers/notetakers/interpreters, special accommodations for test taking needs, assistance with architectural barriers, assistive technology, and support for individual needs.

USC Campus Support and Intervention - (213) 821-4710
campussupport.usc.edu
Assists students and families in resolving complex personal, financial, and academic issues adversely affecting their success as a student.

Diversity at USC - (213) 740-2101
diversity.usc.edu
Information on events, programs and training, the Provost's Diversity and Inclusion Council, Diversity Liaisons for each academic school, chronology, participation, and various resources for students.

USC Emergency - UPC: (213) 740-4321, HSC: (323) 442-1000 – 24/7 on call
dps.usc.edu, emergency.usc.edu
Emergency assistance and avenue to report a crime. Latest updates regarding safety, including ways in which instruction will be continued if an officially declared emergency makes travel to campus infeasible.

USC Department of Public Safety - UPC: (213) 740-6000, HSC: (323) 442-120 – 24/7 on call
dps.usc.edu
Non-emergency assistance or information.