EE354L: Introduction to Digital Circuits

Course Number & Title: **EE354L: Introduction to Digital Circuits**

Units: 4

Semester and time: Spring 2021 semester
https://classes.usc.edu/term-20211/course/ee-354/
Lecture: MW 10:00-11:50 AM on Zoom/in RTH105
Lecture: MW 2:00- 3:50 PM on Zoom/in RTH105
Labs: 4 labs each lab 2H 50M on Zoom/in OHE336
(i) 6:00-8:50 PM Mon. (ii) 5:00-7:50 PM Tues. (iii) 5:00-7:50 PM Wed. (iv) 6:00-8:50 PM Thurs.

Location: Lectures: on Zoom/in RTH105; Labs on Zoom/in OHE336

Instructor: Gandhi Puvvada

Office: on Zoom/in EEB 238 684 224 6098 password: 457354

Office hours: 4 hours per week 4:00-5:00PM MW, 3:00-4:00 PM TTh on Zoom
http://www-classes.usc.edu/engr/ee-s/457/Gandhi_Office_Hours/Gandhi_Office_Hours_Sp2021.pdf

Contact information: gandhi@usc.edu, ~~Office: (213) 740-4461~~, Cell: (310) 733-8025

Catalog Description:
https://catalogue.usc.edu/

EE 354L Introduction to Digital Circuits (4, FaSpSm)
Digital system design and implementation; synchronous design of datapath and control; schematic/Verilog-based design, simulation, and implementation in Field Programmable Gate Arrays; timing analysis; semester-end project. *Prerequisite:* EE 109L. (Duplicates credit in EE 254.)

Learning objectives:

Upon completion of this course students will be able to:
1. Design, simulate, and build (implement on a FPGA board) a substantial digital system
2. Design a digital system using Verilog HDL (Hardware Description Language)
3. Understand RTL design (DPU and CU) and Timing design
4. Understand the use of an embedded processor in a digital system design
5. Compare dedicated hardware implementation with a processor-based implementation
6. Understand an 8-bit processor pinout, address decoding and SRAM memory interface
7. Understand issues with Clock domain crossing, 4-way and 2-way handshake, single-clock and two-clock FIFOs (First-In First-Out buffers) and their application
8. Understand tristate buffers, open-drain devices, buses, bus arbiters, rotating prioritizer
9. Understand how serial busses work, and get to know I2C bus operational details
10. Finally design and implement a semester-end project

Website: https://blackboard.usc.edu/

TAs:
EE354L TA -- Sasindu Kangara Mudiyanselage <kangaram@usc.edu>
EE354L TA -- Chao Wang <wang484@usc.edu>
EE354L TA -- Jing lei Cheng <chen520@usc.edu>

Course Mentors:
The 4 TAs are also Mentors for this course, and they each will hold one hour of office hours per week (TBA).
They can be consulted on both lab and lecture material during the office hours. During the lab, if they are free, they can help you with the lecture material, but the lab material is of importance during the lab time.

Grader: EE354L Grader -- 2 hours per week (TBA) Will help only on lecture material and homeworks.

Office hours: 1. Gandhi 4:00-5:00PM MW, 3:00-4:00 PM TTh on Zoom Gandhi_Office_Hours_Sp2021.pdf
2. TAs' Hours: TBA
Sasindu:
Chao:
Jing lei:
3. Grader : TBA

Prerequisite: EE109
Recommended Preparation: Basic programming skills taught in courses like EE109L (Introduction to Embedded Systems)

Optional Textbook: Digital Design: Principles and Practices, 4/E By John F. Wakerly
http://www.ddpp.com/
Required class-notes and lab manual: Class-notes and Lab Manual distributed online progressively

Recommended Reading: The lecture-by-lecture topic list in the last few pages of this syllabus is tentative and may change substantially as we are changing some labs and remote lab instruction during COVID is challenging. Lecture sequence needs to adapt to the lab sequence. We will maintain a list of lecture topics "taught/to be taught" and convey (through an email) what we are going to cover in the next lecture. Please browse through the pdf files associated with the lecture for 10 minutes so that you are generally aware of the topic and slide sets. After each lecture, please spend at least 20 minutes that night (before you forget) browsing through the covered slides and note down points needing clarification. Discuss those points during our office hours. And, on weekend, please spend an hour or two to completely learn the material of that week's lectures.

Course Material: Class-notes and Lab Manual

EE354L is an intensive design course, reinforcing class-room lectures with homework and lab assignments.
Textbooks often fail to cover the design process adequately. The lecture material and the lab assignments were developed over the last 30 years of teaching this subject. It may look slightly unorganized, but it has all the material. I keep all the past exams open. So, you have abundant practice material available to make use of.

Attendance policy: http://www-classes.usc.edu/engr/ee-s/254/ee354l_attendance.html

Grading Policy (approximate weights) (approximately 47% in assignments and 53% in exams)**:**
Weights vary slightly from semester to semester. Example: Fall 2020 Grade sheet

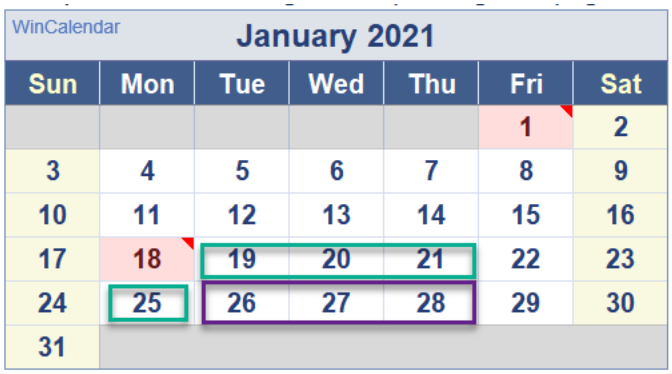
Also, I use two scales (weights) for the three exams to compute the exam total and take the higher of the two for each student, so that if one does poorly in the Quiz+Midterm, he/she can try to do better in the final.

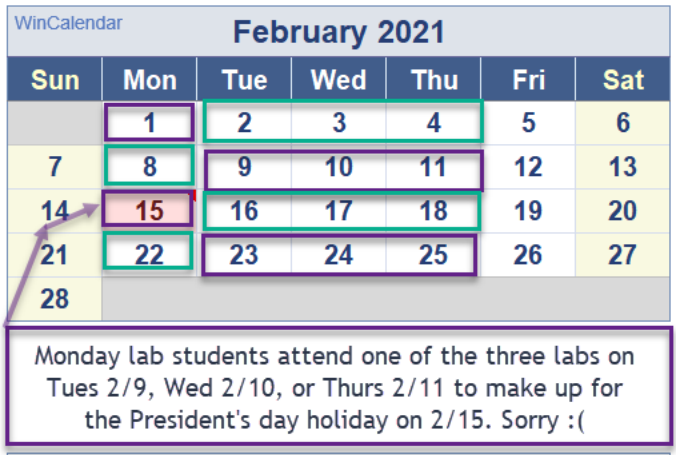
	Weight 1	Weight 2
HW	6.25	6.25
Short Exercises	2.75	2.75
LAB	24.00	24.00
Project	10.00	10.00
TA	3.00	3.00
Quiz	7.50	9.50
MT	19.50	22.50
Final	27.00	22.00
	100.00	100.00

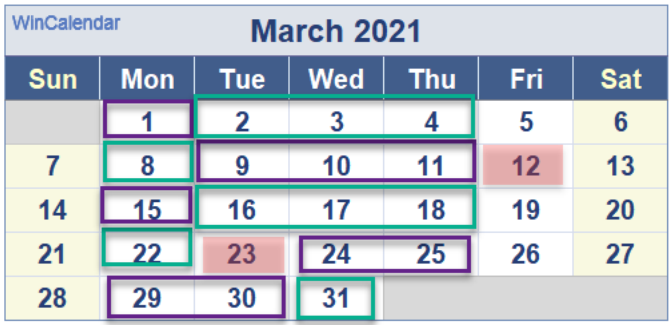
Class Tentative Schedule: Topics and the order of lectures change a lot each semester.
Listed below are tentative dates for the lectures and labs. We will separately maintain a list of topics "taught/to be taught" in **ee354L topics covered in Sp2021.docx** and revise it every week progressively.

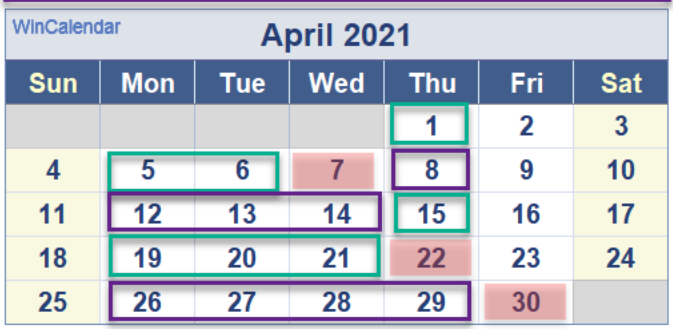
We have four lab sessions every week.

TWTM (in the lab rows below) stands for Tuesday, Wednesday, Thursday and the next Monday. It refers to the four labs every week. Since the first Monday Jan 18, 2021is a holiday, we made the Lab week to start on Tuesday and end on next Monday. For example, the Lab #1 is taught on Tuesday 1/19, Wednesday 1/20, Thursday 1/21 and the next Monday 1/25. While it starts as a TWTM Lab Week for the first 9 weeks, the special "Wellness Day (No classes)" in March and April will alter this for the next 5 or 6 weeks. The last 6 weeks of the semester shrink to 5 lab weeks because of the wellness days. Please see the 14 lab weeks marked in green and purple rectangles on the 15-week semester below. We request the Monday lab students to make up for Feb. 15th holiday as marked below.









Lec/Lab	Date	Day	Topics and Assignments
	January		
	18	Mon	Martin Luther King Day, university holiday calendar
Lec#1	20	Wed	Course intro., Nexys-4 (FPGA Board) Intro. Time-Division multiplexed 7-segment Common Anode Display Nexys4_Basic_IO_Introduction.pdf Nexys_4_documentation/ Vivado_installation/ (Old Nexys 3 pdf pdf .avi)
Lab#1		TWTM	Nexys-3/Nexys-4 (FPGA Board) Intro. Time-Division multiplexed 7-segment Common Anode Display pdf pdf .avi Detour Signal State Machine (Schematic) pdf .avi (Vivado 2019.2 for Synthesis, Modelsim for Simulation, etc.)
Lec#2	25	Mon	DPU & CU (Data Path Unit and Control Unit), One-hot state assignment for CU design pdf .wmv , ME (Mutually Exclusive) and AI (All Inclusive) rules in designing a state diagram pdf .avi ; State diagram Design examples .pdf .avi Detour lab pdf HW#5 Example of One-hot state assignment for CU design pdf dir
Lec#3	27	Wed	Data registers -- clocking and controlling pdf .avi ; Mealy machine example -- Divider Design pdf .avi ,
Lab#2		TWTM	Detour Signal State Machine (Schematic) pdf .avi

	February		
Lec#4	1	Mon	Introduction to the number lock lab. Verilog HDL Introduction pdf .avi , 0_Verilog_Main_Points_of_the_6_Lectures.pdf Verilog introduction, event driven simulation, cycle driven simulation, delta-T associated with non-blocking assignments which is crucial for successful simulation of a zero-delay modeling of a sequential logic (having Flip-Flops) (example: shift register)
Lec#5	3	Wed	Sync_Counter_with_clr_load_en.pdf to illustrate Intercept and Inject method of building data path. .avi To make HDL coding readable and maintainable, there is an important need to reduce number of concurrent items by combining related logic together (example: deep combinational logic, where blocking assignments are important). Verilog Blocking and Non-blocking assignments, RTL coding in Verilog .pdf .avi .zip
Lab#3		TWTM	Verilog Introduction Labs (Synchronous and Asynchronous FF resets, and Divider RTL design in Verilog example design, Divider Moore machine design) .pdf .pdf .avi .pdf .zip
Lec#6	8	Mon	Loop Counter Incrementation and Terminal Value Checking pdf .avi pdf pdf pdf Verilog HDL behavioral modeling pdf .avi Verilog HDL Data types pdf .avi and Sequential Statements pdf .avi
Lec#7	10	Wed	Lab #6a RTL Coding -- Divider Example -- Debouncing, Single-stepping, and output coding pdf & .avi
Lab#4		TWTM	Number Lock State Machine, Nexys-4 Top design, all in Verilog .dir pdf
	15	Mon	President's Day, university holiday calendar **But the Monday lab needs to make up ☹**
Lec#8	17	Wed	State machine design examples
Lab#5		TWTM	Lab #6a RTL Coding -- Divider Example -- Debouncing, Single-stepping, and output coding pdf & .avi

Lec#9	22	Mon	**Picoblaze** The following is a quick introduction to the topics below as a prelude to introducing PicoBlaze in the next lecture. Introduction to Memories, Processors, Processor pinout, Processor Address Map, Byte Addressability, Processor address decoding, I/O addresses, I/O ports, Input port may or may not require a storage register to hold input data before collection by the processor, Output port needs a storage register to hold the output data sent by the processor for display or transmission, Interrupts, Interrupt service routine, sharing a single interrupt request (INTR) pin and identifying the requester. PicoBlaze is not for data crunching, it is meant to provide control sequences to perform a job such as UART, etc.
Lec#10	24	Wed	Picoblaze introduction, Picoblaze Assembly Language, dir pdf pdf pdf 1.mp4 2.mp4
Lab#6		TWTM	GCD (Greatest Common Divisor) design .pdf
	March		
Lec#13	1	Mon	Data-path design (a) small system design .pdf .avi BCD to Binary and reverse conversion Chapter 7 , Inches to Yards-Feet-Inches conversion pdf .avi, GCD design pdf .avi
Lec#14	3	Wed	Quiz preparation
Lab#7		TWTM	Picoblaze introduction, EE354L_Get_acquainted_with_PicoBlaze.pdf .pdf
	6	Sat.	**Quiz (~10%): Saturday, Mar. 6, 2021 04:05-07:40** **(actual exam 04:20-07:20 PM)**

Lec#15	8	Mon	Array processing in RTL, pointers and pointer incrementation, HW#8A .pdf Due dates and info: .pdf Directory .dir
Lec#16	10	Wed	Picoblaze interface to external hardware, input and output ports, ~~Hex Keypad .pdf .pdf .pdf~~ Picoblaze Interrupts .pdf (covered through a pre-recorded 8-part lecture mp4.zip posted at dir)
Lab#8		TWTM	Writing Testbenches .dir .pdf
Lec#17	15	Mon	Timing Design part 1 setup and hold margins, synchronizing asynchronous inputs .pdf HW#8 on Data Path Unit Design .pdf sol.pdf (~~.pdf .wmv.zip~~)
Lec#18	17	Wed	Timing Design part 2 reset synchronization, Shannon's expansion theorem applications .pdf Midterm review, Q#2, ~~Q#3~~ from Sp2013 .pdf sol.pdf [Note:Q#3 is truck off as it deals with a topic, "microprogrammed control unit", which is not being taught in recent years.]
Lab#9		TWTM	Divider_Pico_N4 pdf dir ~~Keypad interface to Picoblaze .pdf~~ , ~~Demo: Divider on Pico .zip~~
Lec#19	22	Mon	Tristate Buffers, muxes and tristate buffers in Data-path design Q#2 MT_Sp12.pdf MT_Sp12_sol.pdf
Lec#20	24	Wed	Decade counter pdf .zip Verilog HDL Blocking and Non-blocking assignments Last two pages pdf pdf .avi Verilog Exam questions review .pdf P1.avi P2.avi
Lab #10		**WTMT (3/24-3/30)**	Picoblaze Interrupts (i) using polling (ii) with no polling Readme dir .pdf
Lec#21	29	Mon	Chapter 11 Memories .pdf .wmv
Lec#22	31	Wed	Slack (make up), Midterm Review
Lab #11		**WTMT (3/31-4/6)**	Timing Analysis and Timing Constraints .pdf Prepare for the semester end project: PMODs, VGA demo, LCD demo, File I/O demo, Logic Analyzer Demo, ChipScope Demo, Final Project proposals

	April		
	3	Sat.	**MT (~22.5%): Saturday, Apr. 3, 2021 04:05-07:40 (actual exam 04:20-07:20 PM)**
Lec#23	5	Mon	Memories lecture completion and FIFO lecture introduction, FIFOs .pdf .wmv
Lab #11		**WTMT (3/31-4/6)**	Timing Analysis and Timing Constraints .pdf Prepare for the semester end project: PMODs, VGA demo, LCD demo, File I/O demo, Logic Analyzer Demo, ChipScope Demo, Final Project proposals
	7	Wed	Wellness Day (No classes) calendar
Lec#25	12	Mon	FIFO completion, Gray code, Binary<->Gray conversion, .pdf , Handshake .pdf .pdf
Lec#26	14	Wed	Make-up lecture
Lab #12		**TMTW (4/8-4/14)**	Final Project proposals approvals, Final Project Week 1
Lec#27	19	Mon	Ch 4_mux, Barrel shifters, priority encoders, Totem-pole and Open-collector output devices dir
Lec#28	21	Wed	~~CLA (Carry Look-ahead Adder) dir~~ or a Make-up lecture
Lab #13		**TMTW (4/15-4/21)**	Final Project Week 2
Lec#29	26	Mon	UART Basics .pdf , I2C Bus Protocol .pdf
Lec#30	28	Wed	Chapter #10 Selected parts of the counter topic -- basics of Ripple and Synchronous counters .pdf Special Counters Exam questions .pdf .pdf .pdf Review for the Final exam (bubble to bubble logic from .pdf)
Lab #14		**MTWT (4/26-4/29)**	Final Project demonstration, presentation, and report submission
	May		
	6	Thursday	Official Final Exam time is as given below. But I am requesting the class to agree to the change proposed further below. ========== https://classes.usc.edu/term-20211/finals/ As per the **Exceptions** schedule at the bottom of the above page. Electrical Engineering 354 Thursday, May 6 8-10 a.m.
	8	Saturday	**Final (~22.5%): Saturday, May 8, 2021 04:05-07:40 (actual exam 04:20-07:20 PM) if everyone agrees to this move the exam to Saturday May 8th from the official Thursday May 6th 8-10 AM.** I have checked the finals schedule and found no conflicts with the proposed time.

Continued on the next page

Statement on Academic Conduct and Support Systems

Academic Conduct:

Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in SCampus in Part B, Section 11, "Behavior Violating University Standards" policy.usc.edu/scampus-part-b. Other forms of academic dishonesty are equally unacceptable. See additional information in SCampus and university policies on scientific misconduct, policy.usc.edu/scientific-misconduct.

Support Systems:

Counseling and Mental Health - (213) 740-9355 – 24/7 on call

studenthealth.usc.edu/counseling

Free and confidential mental health treatment for students, including short-term psychotherapy, group counseling, stress fitness workshops, and crisis intervention.

National Suicide Prevention Lifeline - 1 (800) 273-8255 – 24/7 on call

suicidepreventionlifeline.org

Free and confidential emotional support to people in suicidal crisis or emotional distress 24 hours a day, 7 days a week.

Relationship and Sexual Violence Prevention Services (RSVP) - (213) 740-9355(WELL), press "0" after hours – 24/7 on call

studenthealth.usc.edu/sexual-assault

Free and confidential therapy services, workshops, and training for situations related to gender-based harm.

Office of Equity and Diversity (OED) - (213) 740-5086 | Title IX – (213) 821-8298

equity.usc.edu, titleix.usc.edu

Information about how to get help or help someone affected by harassment or discrimination, rights of protected classes, reporting options, and additional resources for students, faculty, staff, visitors, and applicants.

Reporting Incidents of Bias or Harassment - (213) 740-5086 or (213) 821-8298

usc-advocate.symplicity.com/care_report

Avenue to report incidents of bias, hate crimes, and microaggressions to the Office of Equity and Diversity |Title IX for appropriate investigation, supportive measures, and response.

The Office of Disability Services and Programs - (213) 740-0776

dsp.usc.edu

Support and accommodations for students with disabilities. Services include assistance in providing readers/notetakers/interpreters, special accommodations for test taking needs, assistance with architectural barriers, assistive technology, and support for individual needs.

USC Campus Support and Intervention - (213) 821-4710

campussupport.usc.edu

Assists students and families in resolving complex personal, financial, and academic issues adversely affecting their success as a student.

Diversity at USC - (213) 740-2101

diversity.usc.edu

Information on events, programs and training, the Provost's Diversity and Inclusion Council, Diversity Liaisons for each academic school, chronology, participation, and various resources for students.

USC Emergency - UPC: (213) 740-4321, HSC: (323) 442-1000 – 24/7 on call

dps.usc.edu, emergency.usc.edu

Emergency assistance and avenue to report a crime. Latest updates regarding safety, including ways in which instruction will be continued if an officially declared emergency makes travel to campus infeasible.

USC Department of Public Safety - UPC: (213) 740-6000, HSC: (323) 442-120 – 24/7 on call

dps.usc.edu

Non-emergency assistance or information.