

USC Viterbi School of Engineering

EE 457 Computer Systems Organization

Units: 4

[Spring 2021](#) - Tues. Thurs. 5:00-6:50PM in OHE136

Instructor: Gandhi Puvvada

Office: Zoom/EEB 238

4 hours per week 4:00-5:00PM MW, 3:00-4:00 PM TTh
on Zoom [Gandhi Office Hours Sp2021.pdf](#)

Contact Info: gandhi@usc.edu,

Office phone: ~~(213)~~ 740-4461,

Cell phone: (310) 733-8025

Teaching Assistant:

EE457 TA -- Kartik Lakhotia <klakhoti@usc.edu>

Mentor: TBA

Office: Zoom/PHE330: Office Hours of TAs and Mentors
TBA

1. Course Description

This course covers computer organization and design. It provides CS/CE/EE students with a substantial understanding of a CPU at its logic design level. Design of the control unit and the data path unit of a simple multi-clock-cycle CPU and a pipelined CPU is covered in detail. Computer arithmetic and memory hierarchies (cache, main memory, virtual memory) are also covered. Hardware support for exceptions, dynamic scheduling of instructions (Tomasulo algorithm to execute instructions in an out-of-order fashion), branch prediction, multi-threaded cores, multi-core processors with cache coherency, locks and mutual exclusion among threads via special atomic instructions are also discussed in detail. Students design in Verilog and use ModelSim simulator to verify their RTL design/simulation exercises.

2. Learning Objectives

At the end of the course, students are expected to feel confident to perform logic design of a CPU or any hardware system utilizing pipelining and other RTL techniques and proceed to graduate courses in computer architecture or general hardware design. This course is also expected to improve students' design skills and analytical skills.

3. Course administration

a) Course prerequisites: EE354L (previously EE254L or EE201L) Introduction to Digital Circuits is a *necessary* prerequisite. Undergraduate students without this prerequisite will not be able to do this course. Graduate students are expected to have taken a logic design course and a course covering some assembly language in their undergraduate course work before taking this course.

Recommended Preparation: Familiarity with the following items at an introductory level is expected.

1. Programming in an assembly language of any processor (CISC or RISC)
General Purpose Registers, Program Counter, Conditional branches, Call and Return instructions involving stack operations, exceptions and interrupts
2. Digital Logic design at RTL level (Register Transfer Language Level)
Small System Design involving a Datapath unit and a Control Unit, ALU design, Timing Design, Waveform drawing and interpretation
3. Design entry using Verilog HDL (Hardware Description Language) and simulation
Event-driven simulation and the delta-T concept, representation of concurrency using instantiations, concurrent *assign* statement, *always* procedural blocks, use of blocking and non-blocking assignments in procedural blocks (blocks with a *begin* and an *end* where sequential statements are used), Testbenches

b) **Classes:** <https://classes.usc.edu/term-20211/course/ee-457/>

Discussion class is *not optional*. Homework and lab assignments are primarily discussed during the discussion class. Important additional material may be covered in the discussion class.

c) **Examinations: No makeup exams.**

Please note that EE457 exams are long (3 Hours) as they are design exams.

One quiz (~11%), one midterm (~24.5%), and the final exam (~33.5%)

The “Quiz” slot (Qz **TBA** → Saturdays 5-8:00PM) (with remote exam on zoom related overhead: 4:45-8:20 PM)

I request all of you to please agree to this Saturday evening time for our quiz and midterm exams so that there is least inconvenience/time conflict caused. I chose evening time so that it is not an odd time for the 12 students in China and the 2 students in India. I do not know the spread of the remaining students across the USA, but I am hoping that the proposed time suits all time zones within the USA.

Quiz (about 11%): Saturday Feb. 20, 2021 05:00 PM - 08:00 PM PST (with remote exam on zoom related overhead: 4:45-8:20 PM)

Midterm (about 24.5%): Saturday Mar. 27, 2021 05:00 PM - 08:00 PM PST (with remote exam on zoom related overhead: 4:45-8:20 PM)

Feb 5 (Friday)? Please verify	Last day to drop a class without a mark of “W”
March 5 (Friday) ? Please verify	Last day to drop a class with a mark of “W”
April 3 (Friday) ? Please verify	Last day to drop a class with a mark of “W”

<https://classes.usc.edu/term-20201/calendar/>

Note: EE457 Final Exam is listed under the Exceptions Schedule posted at the bottom of:

<https://classes.usc.edu/term-20211/finals/>

Electrical Engineering 209, 457 **Wednesday, May 12** **4:30-6:30**

I propose that the time is extended to 7:30 PM as shown below to allow a 3-hour exam.

Final Exam (about 33.5%): Wednesday, May 12, 2021, 4:30 PM - 7:30 PM PST (with remote exam on zoom related overhead: 4:15-7:50 PM)

Official slot is 4:30 PM to 6:30 PM. With your cooperation, I want to extend it by 1 hour by ending the exam 1 hour late. Further, when we include the overhead due to this semester’s online exam on zoom, we need to make sure that you are available from 4:15 to 7:50 PM. I have checked the final exam schedule and noted that CSCI170 and CSCI270 will conflict with my final exam as their final exam is on the same day from 7 PM to 9 PM. I am hoping that none of our EE457 students are taking those courses. We will reconfirm with all our students to make sure that this works for everyone. Please let me know if you face any undue hardship or time conflict because of this time extension.

d) **Grading Policy:**

Course weights		
Assignments	percentage	Late submission penalty for assignments
Homeworks (short and long) (Individual work)	about 6% to 11%	5% penalty per day for long homeworks up to 1 day if solution is not given out. For short homeworks, solution is given away at the time of the assignment. 5% penalty per day for one day for short homeworks also.
Labs (Teamwork)	about 22% to 24%	3% flat penalty up to 3 days
Exams	Scale1 Scale2	

Quiz	10%	12%	no make-up exam
Midterm	22%	27%	no make-up exam
Final	37%	30%	no make-up exam
Attendance is noted based on Zoom meeting participation lists (they show time joined and time left!)			
Penalty for lecture absence: 1% of the course for the 4th and the 5th; 2% for the 6th and thereafter			
Penalty for discussion absence: 0.5% for the 4th and the 5th; 1% for the 6th and thereafter			

e) Academic Accommodations:

Any student, requiring academic accommodations based on a disability, is required to register with the Center for Academic Support and Disability Services and Programs (CAS & DSP) each semester.

An online profile can be created on [MyDSP](#).

A letter of verification for approved accommodations can be obtained from CAS & DSP.

Please make sure that the letter is delivered to me as early in the semester as possible (no less than **2 weeks** before an exam).

The CAS & DSP office is located in GFS 120.

Their phone number is (213) 740-0776. Email: DSPPFrontDesk@usc.edu

<https://dsp.usc.edu/new-to-dsp/main-facilities/>

f) Miscellaneous administrative matters:

Lecture class attendance, penalty for absence, and minimum required performance:

If you miss more than 2 lecture meetings, you will start noticing that you are falling behind.

If you miss more than 5 lecture meetings, you may as well drop the course.

It is a design course requiring continuity in your learning process. So, please attend every lecture/discussion meeting.

Attendance is noted based on Zoom meeting participation lists (they show time joined and time left!)

Penalty for lecture absence: 1% for 4th, 5th; 2% for 6th and after.

Penalty for discussion absence: 0.5% for 4th, 5th; 1% for 6th and after.

http://www-classes.usc.edu/engr/ee-s/457/EE457_attendance_policy.html

The remote students are allowed to watch the lecture in the evening/late night. But they should finish watching lectures of a week within that week and send an email to the instructor/TA stating that they watched the week's lectures and discussion before the next Monday.

Homeworks and *short exercises posted on D2L* shall be done individually. ~~*In-class exercises (but not short exercises posted on D2L) can be done taking help from fellow students but each student shall submit individually his/her completed work.*~~ Design and simulation labs can be performed either individually or in teams of two students (2 per team). But occasionally, design labs may be assigned as individual assignments.

Teams shall submit only one set of Verilog code and results online.

However, justifications/explanations, state diagrams, and answers to questions at the end of the lab assignment (paper submissions), shall be prepared individually.

Copying is different from discussing ideas with other students.

You are encouraged to share your thoughts on all items of the course (homework, design labs, and design lab reports) with other students as long as one of you act as a *Teaching Assistant* who tries to help without giving away the solution. Of course, exams are completely individual (I do not need to say this, but ..).

Absolutely no copying. Do NOT try to copy any assignment. We have ways to find if a design/simulation lab or a homework has been copied.

Try not submitting a non-working lab as we give very little credit for a non-working lab.

We are here to help you and guide you in your debugging. If you submit a **non-working design/lab** and if you do not write on the top of it in **BIG** letters that it is NOT WORKING (and further do not inform the instructor/the TA, and the lab graders through an email before submission), we will treat it as an attempt to cheat. This is very important.

Academic dishonesty cases will be dealt with severely. Please go through the short tutorial on Academic Integrity at USC posted at

<https://libraries.usc.edu/research/reference-tutorials>

Try to see which version works for you (one with _html5 and the other without)

<http://lib-php.usc.edu/libraries/about/reference/tutorials/avoiding-plagiarism/story.html>

http://lib-php.usc.edu/libraries/about/reference/tutorials/avoiding-plagiarism/story_html5.html

Also please go through <http://usclibraries.adobeconnect.com/academicintegrity>

Also please go to <https://myviterbi.usc.edu/> and watch a video on Academic Integrity Introduction.

Another important resource is the Student Judicial Affairs and Community Standards (SJACS) website .

Please go through the guidelines for academic integrity review process, which can be found in the Student Conduct Code in the current SCampus at <https://policy.usc.edu/student/scampus/>, Part B, Section 13 (**Section 13 – Academic Integrity Review**). Please familiarize yourself with these standards and expectations concerning academic integrity. University policy requires that all academic integrity violations are reported to Student Judicial Affairs and Community Standards (SJACS) if the student is an undergraduate and to the VSoE if the student is a graduate student.

We will try to make the assignments due on times far from the class time.

This is to make sure that students do not miss classes to complete their assignments.

Please check your email regularly. Also visit the DEN D2L regularly at <https://courses.uscdcn.net/>

D2L stands for Desire2Learn, a Learning Management System used by DEN.

<https://gapp.usc.edu/graduate-programs/den/technical-support/Desire2Learn>

<https://viterbigrad.usc.edu/technical-support/course-management-system/>

4. Design/simulation labs sequence:

Example Weights of the labs: Note that some labs have zero weights as you are not asked to submit these labs.

However, you may still be responsible for reading the lab, understand the design, and are able to answer questions on these items also on the exams. Please refer to the exam-preparation guide sent to you before each exam regarding labs with zero weight. Labs and HWs vary slightly from semester to semester. The list below is from a recent semester [Fall 2020](#).

RTL LABS		
#	Points	weight
1P1	100	0.50
1P2	100	0.70
1P3_M1	100	0.60
1P3_M2	100	0.60
1_Paper	100	0.60
FIFO_P1	100	0.60
FIFO_P2	0	0.00
ALU LABS		
3	100	0.80
3_paper	100	0.60

CPU LABS		
4P4	0	0.00
6P4	100	1.10
6P5	100	0.00
7P1	100	0.00
7P1&P2 Paper	100	1.20
7P3_SP1&2 Paper	100	1.20
7P3_SP1	100	1.20
7P3_SP2	100	0.00
7P3_SP3	100	1.20
7P3_SP4	0	0.00

Approximately one lab (or one part of one lab) will be assigned every week starting from the second week. The labs make up about **22%** of your course credit.

0) Introduction to Verilog HDL entry and simulation in Modelsim

1) Max. Min. finder State Machine Design Lab #1 Part #1, Part #2, Part #3 (M1, M2, ~~M3~~, M4)

2) Design of a 32-bit ALU Lab #3

3) FIFO ~~and its application~~

4) ~~Multi-cycle CPU Design Lab #4 Part #4 (only paper submission)~~ <= not covered in the short semesters Fall 2020 and Spring 2021

5) Pipeline labs

Design of a 3-element adder Lab #7 Part #1, #2,

Design of a simple pipeline Lab 7 Part #3 (Sub parts SP1, SP2)

RTL Coding of a simple pipeline Lab 7 Part #3 (Sub parts SP3, ~~SP4~~)

6) Design of a Pipelined CPU Lab #6 Part #4 and Part #5 (only paper submissions)

5. Readings:

The required readings are class notes and sections of the textbook. Please make it a practice to read regularly. It is important to clarify any items that are not clear in that week itself. Students, who postpone reading, gradually drift away from the rest of the class and eventually perform very poorly on the exams and design/simulation labs.

Primary References:

Class Notes (required): Please buy from the university (USC) bookstore. Please access it [online](#).

Lab Manual: Individual labs are posted on the ee457 D2L page.

Textbook/Verilog Guide:

1. [Computer Organization & Design](#) - The Hardware and Software Interface 5th edition

By D. A. Patterson (Berkeley) and J. L. Hennessy (Stanford)

We do not use the textbook that much. Some students manage without the textbook. But this is a very good book to buy and keep.

You can buy it from the university (USC) bookstore or any place (such as online bookstores).

<http://store.elsevier.com/Computer-Organization-and-Design/David-Patterson/isbn-9780124077263/>

If you have the 4th edition, that is fine too.

2. The Verilog 2001 Reference Guide by Esperan (Cadence)

You need this for your Verilog-based design/simulation labs. **You can use it in the EE457 exams.** Esperan (Cadence) does not sell it to individuals. They provided the pdf file to us free. It is posted on the D2L. Please do not redistribute or repost it anywhere. We will bring a few printed copies to the exam hall and you can borrow a copy for a short time.

Secondary References (Do not buy these):

1. EE101 and EE354L (EE254L) Textbook: Digital Design Principles and Practices by John F. Wakerly

2. EE557 Textbook: Parallel Computer Organization and Design by Dubois, Annavaram, and Stenstrom

3. Computer Architecture - A Quantitative Approach by D. A. Patterson and J. L. Hennessy

6. Course Schedule by week for Spring 2021:

Chapter numbers point to chapters in my class notes (http://www.classes.usc.edu/engr/ee-s/457/EE457_Classnotes/).

Homeworks and labs are due generally 1 week after they are assigned.

Due dates calendar has been posted.

# of lectures	Lecture #	Item	Homework /Lab
2	1, 2 Week #1 1/19-1/21	Ch#1 Intro to course, review of prerequisite material, Review data path and control unit design, Moore and Mealy, Glitches in control signals, Data registers with Data enable, State diagram design, All Inclusive and Mutually Exclusive rules, Concurrent RTL operations in RTL design. welcome.pdf , 1_microarchitecture.pdf , DPU_CU.pdf , 3_Moore_Mealy_Divider.pdf , 4_Data_Registers.pdf , 5_P1_loop_counter.pdf , 5_P2_loop_counter.pdf , 5_P3_loop_counter.pdf , 6_P1_mutually_exclusive.pdf , 6_P2_ME_AI_tables.pdf , 7_State_Diagram_Design_examples.pdf	HW#1 H1.pdf RL.pdf HW#1A for practice H1A.pdf HW1A_sol.pdf
0		Verilog coding: Watch the 6-part EE354L lectures at home and learn by yourselves. Install Modelsim/Questasim and learn to use the tool by yourself	Tools installation and/or VDI
1	3 Week #2 1/26-1/28	Compare and contrast: state diagram vs. flow-chart, Min-Max (a 4-part lab: P1, P2, P3-Method1, P3-Method-3)	Lab #1
1	4 Week #2 1/26-1/28	Ch#2 Performance, MIPs, MFLOPs ch2.pdf Amdahl_Law.PDF	HW #2 HW2.pdf
2	5, 6, Week #3 2/2-2/4	Ch#3 MIPs ISA, SLT, SLTU lw, sw, Byte addressable processors, memory addresses. also cover word addresses in a byte addressable processor P1.pdf , P2.pdf , addr_space_exer.pdf , addr_space_sol.pdf , Quiz_Sp2019_sol_Q4 (.pdf, .mp4) HW#3 (exer.pdf , sol.pdf , disc.pdf , disc.avi) HW4page2.pdf	HW#1B HW1B.pdf
1	7, 8 Week #4 2/9, 2/11	Ch#4 P1 Review overflow detection in unsigned and signed arithmetic and ALU design P1.pdf , alu.pdf , ee560_HW0_ques_adder.pdf MT compare	ALU lab .pdf .pdf Lab #3 .avi .zip
2	8, 9 Week #4, 5 2/11, 2/16	Ch#5 P1 Single Cycle CPU, ch5_p11.pdf ch5_p12.pdf dp1.pdf dp2.pdf dp2_blank.pdf HW#5a intro .pdf .avi	HW #5A (Single-cycle CPU)
1	10 Week #5 2/18	Ch#7 P1 Cache: Mapping techniques, CPU address division into fields and connect address p1.pdf bookshelf .pdf .avi .pdf .mp4 MT Cache reverse engineering ques.pdf sol.pdf Review for the Quiz items from prep guide .pdf signed/unsigned numbers comparison: Q2 of Fall 2018 Quiz exam.pdf sol.pdf	Cache HW #6 (page 1 only) .pdf sol_page1.pdf
	Week #5 2/20	Quiz exam on Saturday Feb. 20, 2021 5:00 PM-8:00 PM on Zoom (with remote exam on zoom related overhead: 4:45-8:20 PM)	Quiz slot was moved to Saturday evening

2	11, 12 Week #6 2/18-2/20	Ch#5 P2 multi-cycle CPU Datapath and control design Ch#5 P2 Multi-cycle CPU 2nd edition design	Lab 4 Part #4 (Multi-cycle CPU) (paper submission) HW #5B (Multi-cycle CPU)
4	11,12, 13, 14 Week #6,7 2/22,2/24, 3/2,3/4	Ch#6 5-stage pipeline: data dependency solutions (Compiler solution, HDU & FU), and branch implementations (late branch vs. early branch), branch delay slots. But cover exceptions later. topics links.pdf review.pdf	FIFO .pdf .wmv lab.pdf lab.zip Pipeline lab #7 P1 and P2 paper .pdf .avi .avi .pdf
2	15, 16 Week #8 3/9-3/11	Ch#7 P1 Cache: Mapping techniques, CPU address division into fields and connect address to Cache Data RAMs, Cache Tag RAMs. p1.pdf p2.pdf HW#6.pdf	Cache HW #6 Lab 6 – Part 4 (paper submission) dir .pdf part5.pdf
	Week #10 3/16-3/18	Spring Recess March 15-19	
		Wellness day, March 12, 2021, Friday USC Academic Calendar	No discussion
2	17,18 Week #9 3/16-3/18	Ch#7 P2 Virtual memory: Multi-level page table, PTBR, principle of inclusion. TLBs, and interleaved main memory lec.pdf x86_PT.pdf MT_4L_PT_Q.pdf MT_TLB_Q.pdf	Virtual Memory HW #7 HW7.pdf
		Wellness day, March 23, 2021, Tuesday USC Academic Calendar	No lecture
1	19 Week #10 3/25	Midterm Review midterm_prep_guide.pdf	
	Week #10 3/27	Midterm exam on Saturday March 27, 2021 5:00 PM-8:00 PM on Zoom (with remote exam on zoom related overhead: 4:45-8:20 PM)	Quiz slot was moved to Saturday evening

1	20 Week #11 3/30	Exceptions (in discussion) Branch Prediction , 1-bit and 2-bit predictors, BPB, BTB overview.pdf loC.pdf lect.pdf RAS.pdf	
2	21, 22 Weeks #11,#12 4/1-4/6	Out of order execution and Tomasulo Part 1 (loI_OoE_OoC), WAR and WAW hazards in OoO execution, IFQ (Instruction prefetch queue), dispatch unit, issue queues, issue unit, CDB, ROB OoC.pdf Old_OoC.pdf loC.pdf Tomasulo_P1.pdf	Lab #7 P3 Sub Parts 1, 2 (paper submission) lab.pdf paper.pdf intro.avi intro.pdf
2	23,24 Weeks #12,#13 4/8-4/13	Tomasulo Part 2 (loI_OoE_loC), ROB, ROB search, Speculative execution and selective flushing if branch was mispredicted, exception handling, loC.pdf Old_loC.pdf OoC.pdf Tomasulo_P2.pdf ROB.pdf	ROB-lab
2	25, 26 Weeks #13,#14 4/15-4/20	Ch#9 Parallel processing, semaphores, Read-Modify-Write (RMW) race, atomic operations on shared variables, CMP, Snoopy Cache Coherency protocols, Write-through vs. write-back, MSI, MOESI MIMD-Carpentry.pdf lect.pdf cache-coherency.pdf cache-coherency.avi Mutual-Exclusion.pdf	Pipeline RTL coding lab Lab #7 P3 Sub Parts 3, 4 lab.pdf lec-slides.pdf lec.wmv 1.zip 2.zip
		Wellness day, April 22, 2021, Thursday USC Academic Calendar	No lecture
1	27 Week #15 4/27-4/29	CMT , Thread-level parallelism, non-blocking cache, MPI overview.pdf lec.pdf 560_CMP_CMT.pdf SMT_Block_diagram.pdf	
1	28 Week #15 4/27-4/29	Locks , Atomic operations, LL and SC instructions in MIPS Mutual-Exclusion.pdf	
		Wellness day, April 30, 2021, Friday USC Academic Calendar	No discussion
		Classes end on April 30, 2021 Friday. Study Days May 2-5 USC Spring 2021 calendar	
		Final exam on Wednesday, May 12, 2021 4:30 PM to 7:30 PM PST Official slot of 4:30-6:30 PM extended by 1 Hour. Please see the exceptions list at the bottom of https://classes.usc.edu/term-20211/finals/ Electrical Engineering 209, 457 Wednesday, May 12 4:30-6:30	Final exam slot extended by one hour

Statement on Academic Conduct and Support Systems

Academic Conduct:

Plagiarism – presenting someone else’s ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in SCampus in Part B, Section 11, “Behavior Violating University Standards” policy.usc.edu/scampus-part-b. Other forms of academic dishonesty are equally unacceptable. See additional information in SCampus and university policies on scientific misconduct, policy.usc.edu/scientific-misconduct.

Support Systems:

Counseling and Mental Health - (213) 740-9355 – 24/7 on call
studenthealth.usc.edu/counseling

Free and confidential mental health treatment for students, including short-term psychotherapy, group counseling, stress fitness workshops, and crisis intervention.

National Suicide Prevention Lifeline - 1 (800) 273-8255 – 24/7 on call
suicidepreventionlifeline.org

Free and confidential emotional support to people in suicidal crisis or emotional distress 24 hours a day, 7 days a week.

Relationship and Sexual Violence Prevention Services (RSVP) - (213) 740-9355(WELL), press “0” after hours – 24/7 on call
studenthealth.usc.edu/sexual-assault

Free and confidential therapy services, workshops, and training for situations related to gender-based harm.

Office of Equity and Diversity (OED) - (213) 740-5086 | Title IX – (213) 821-8298
equity.usc.edu, titleix.usc.edu

Information about how to get help or help someone affected by harassment or discrimination, rights of protected classes, reporting options, and additional resources for students, faculty, staff, visitors, and applicants.

Reporting Incidents of Bias or Harassment - (213) 740-5086 or (213) 821-8298
usc-advocate.symplicity.com/care_report

Avenue to report incidents of bias, hate crimes, and microaggressions to the Office of Equity and Diversity | Title IX for appropriate investigation, supportive measures, and response.

The Office of Disability Services and Programs - (213) 740-0776
dsp.usc.edu

Support and accommodations for students with disabilities. Services include assistance in providing readers/notetakers/interpreters, special accommodations for test taking needs, assistance with architectural barriers, assistive technology, and support for individual needs.

USC Campus Support and Intervention - (213) 821-4710
campussupport.usc.edu

Assists students and families in resolving complex personal, financial, and academic issues adversely affecting their success as a student.

Diversity at USC - (213) 740-2101
diversity.usc.edu

Information on events, programs and training, the Provost’s Diversity and Inclusion Council, Diversity Liaisons for each academic school, chronology, participation, and various resources for students.

USC Emergency - UPC: (213) 740-4321, HSC: (323) 442-1000 – 24/7 on call

dps.usc.edu, emergency.usc.edu

Emergency assistance and avenue to report a crime. Latest updates regarding safety, including ways in which instruction will be continued if an officially declared emergency makes travel to campus infeasible.

USC Department of Public Safety - UPC: (213) 740-6000, HSC: (323) 442-120 – 24/7 on call

dps.usc.edu

Non-emergency assistance or information.