3/4/2019

An invitation to join EE560 in Summer 2019

Dear EE MS/PhD students and EE/CECS undergraduate students,

Subject: EE560 in Summer 2019 -- an invitation to join this exciting course

http://classes.usc.edu/term-20192/classes/ee-560
http://classes.usc.edu/term-20192/calendar/
http://classes.usc.edu/term-20192/codes/

The EE560 course is a 4-unit 10-week on-campus summer course running from 5/15/2019 Wednesday to 7/24/2019 Wednesday in Summer 2019). There are two lecture (MW and TTh) sections and one lab section (Tu). We will increase the total capacity to 90 (= 45 * 2) if needed. We will accommodate all qualified students.

The session code is 906. An extract from http://classes.usc.edu/term-20192/codes/ :

Session	Session Length (weeks)	Classes Begin	Last Day to Drop with refund	Last Day to Drop w/o a "W"	Last Day to Drop with a "W"	Classes End	Finals End
906	10	5/15/2019	5/28/2019	6/11/2019	7/10/2019	7/24/2019	7/24/2019

The lab section on Tuesday is common to both the lecture sections. The midterm and the final exams are common to both the lecture sections and are held on the following days.

Midterm Exam July 3, 2019 Wednesday 2:00-5:50PM (lecture class extended)
Final Exam July 24, 2019 Wednesday 2:00-5:50PM (lecture class extended)

Lectures on Monday and Tuesday before the Wednesday exam (Midterm or the Final): In those two exam weeks, I request both MW and TTh sections to attend the Monday lecture which is included in the Wednesday exam.

Please do not plan any travel during the 10-week term (not even for the July 4th weekend). Also, please do not try to travel between the end of Spring 2019 and the start of Summer 2019. It is too short. I will not allow students to join EE560 even 1-day late. The is a substantial penalty for absence in lecture or lab.

Please plan your travel on or after July 25, 2019 Thursday night so as to leave one day extra after the final exam to complete the demonstration of your last project if you run into problems in demonstrating it before the final exam. As per https://academics.usc.edu/calendar/academic-calendar-2019-2020/ the Fall 2019 classes begin on August 26th. So, you will have good vacation of 4 weeks at the end of the Summer 2019.

Extract from the Summer 2019 University Calendar http://classes.usc.edu/term-20192/calendar/

May 27, 2019	**Monday**	**Memorial Day**	**University Holiday**
July 4, 2019, July 5, 2019	**Thursday, Friday**	**Independence Day**	**University Holidays**

The Tuesday May 28th lecture will be recorded so that the MW class can make up for the May 27th holiday. Since the material is vast, and since we lose two lectures because of the exams and one day for the Independence Day holiday, for the first few weeks of the 10 weeks, we will extend our lectures to 5:10PM (with two 8-minute breaks) so that you are ready to do your labs/projects.

The EE560 course (Digital System Design course) deals with hardware architecture and implementation of fairly complex hardware systems. It builds upon the pipelined CPU architecture taught in EE457 and tries to teach digital design detailing and implementation techniques. Too often we come across graduate students who can only *talk* about hardware design but cannot *implement* even a simple 5-stage CPU. At USC, we want our students to be able to design and implement (at RTL level) *whatever* they can architecturally imagine. EE560 tries to achieve this ambitious goal through carefully designed labs and projects. Several DR (Directed Research) students and TAs have worked with me in the past 25 years on these EE560 labs/projects.

The major three design and implementation projects are (i) out-of-order instruction-executing CPU (ii) multi-threaded multi-core CPU and (iii) PCIe (PCI express) Datalink layer and Physical layer (logical). Besides these, the EE560 covers VHDL, Verilog, FPGA Synthesis, timing design, and several system design issues. Topics include simple mesh network for processor-memory communication following AXI protocol, FIFOs, Synchronous SRAMs, Synchronous DRAMs, latch-based pipeline with slack borrowing/time stealing, non-linear pipeline design, gated clocking, cache/CAM design, UART, ChipScope (the on-chip logic analyzer), File I/O between the PC and user board, etc.

The lab/project designs are provided to you in 70% completed form for you (and your team mate) to complete the remaining 30%. However, you need to understand the complete 100% of the design and hence you will be able to explain your design to your interviewers. For most of the designs, besides testing and proving them in simulation, you also implement them on a FPGA, and finally test them on the FPGA board (Nexys-4 with Xilinx Artix-7 FPGA).

Some details about the three major projects:

1. An **OoO Tomasulo processor**: It executes instructions in out-of-order by scheduling instructions ready for execution dynamically. It performs speculative execution through branch prediction and in-order commitment through a reorder buffer (ROB). It flushes junior instructions in the backend (and in the reorder buffer) in case a branch is found to be mispredicted. It has a Physical Register File (PRF) (different from architectural register file), a Free Register List (FRL), a F_RAT (Front-end RAT (Register Alias Table)), and a Checkpoint mechanism to quickly recover after a branch misprediction. Physical register Files, Free Register Lists, RATs (Register Alias Tables) and check pointing mechanisms are used in many current processors from Intel and others.

2. A **4-core processor** with each core running 4 threads: It supports MOESI cache coherency and mutual exclusion via locks in shared memory. MIPs LL (Load-Linked) and SC (Store-Conditional) instructions provide mutual exclusion and synchronization. Non-blocking cache with MSHRs (Miss Status Handling Registers) and Snoopy control unit are implemented to support execution of the remaining threads while some threads have experienced cache misses.
CPU is tested with example assembly language codes running on the 16 threads and interacting through shared memory locations using two methods (i) with locks and (ii) without locks (lock-free).

3. PCIe (**PCI express**) Students design parts of the Physical Layer (Logical) and Data Link Layer. Students learn LTSSM, 8B/10B encoding and decoding, elastic buffer design, Lane_to_lane_deskewing, Data Link Layer and Ack/Nack protocol. They design parts of the system, integrate the system, and test and understand how to verify critical parts of the design using Chipscope (Xilinx's on-chip logic analyzer) at runtime.

Tentative approximate weights	
Homeworks	**5 to 10%**
Labs and projects	**45 to 40%**
Midterm	**25 to 20%**
Final Exam	**25 to 30%**

Xilinx Synthesis tools and Modelsim/Questasim HDL simulation tools will be used. A Xilinx FPGA board (Nexys 4 board with Artix 7 FPGA XC7A100T from Digilent Inc.) will be used for implementing designs. Do not buy the board yourself. We will lend it to you.

Selection criterion and D-clearances

Students with an "**A-**" grade or better in any of the five courses EE457, EE557, EE577a, EE577b, and EE 533, in recent semesters including the current Spring 2019 semester, are eligible to join EE560. Also, students with **two** "**B+**" grades in any two of the same five courses are eligible to join EE560. If a student qualifies through his/her grade in a course other than EE457, he/she is still responsible for the material covered in EE457.

Students meeting the above qualification may submit their D-clearance request online through the online d-clearance system (which can be accessed via My Viterbi at http://myviterbi.usc.edu) starting from Tuesday 3/4/2019. They need to indicate how they satisfied our selection criterion by stating in which semester(s) they obtained the qualifying grade(s) in which subject(s) in the box at the bottom of the **D-Clearance and Pre-Requisite Waiver Request Manager** form. An image of the box is shown below.

If you are requesting D-Clearance for a 500 or above course, please list below when you took the prerequisite or placement exam:

They will get an email from the department in a day or two stating that they were given the D clearance. We will distribute students across the two sections (MW and TTh) and you may or may not get your choice of the section. We will however allow mutual exchange between two students in different sections which will not upset the balance between the two sections.

We will release about 40 D-clearances in the first 8 weeks of registration. Then we will wait until May 13th for the current Spring semester students to receive their grades (http://classes.usc.edu/term-20191/finals/).
The D-clearances will EXPIRE in about 1 week initially and in 2 days in May. If you are given a D-clearance and if you later change your mind and do not wish to take EE560, please go to EEB 102 and get your D clearance cancelled so that your seat can be given to another student. If a student does not register by the D-clearance expiration date, we will assume that he/she does not wish to join EE560 any more.

We will continue to give D clearances until Tuesday May 14th, for the current Spring 2019 students.
We hope the above procedure is fair to all. You should not fear that seats will be gone because even though there are several qualified students, Summer session may not be convenient to them. And, if needed, we will try to increase the capacity to 90 (45+45=90).

Workload

The workload is high (1.5 times that of ee457) and only students, who enjoy design (and who would not mind the time it takes), will like the course. Please do not plan any travel during the 10 weeks. You may want to plan your travel only after July 25th Thursday night to allow 1-day extra time if needed to complete demonstrating your final project.

I am excited at the prospects of teaching a great set of students.

Cheers
Gandhi

p.s. If a student has not taken EE457/EE557 here at USC but is qualified to take EE560 through other courses, I advise that he/she attends one of the two TTh lectures of the current (Spring 2019) EE457 for the last 5 weeks of Spring 2019 to acquaint with Branch prediction, OoO (Out of Order) execution, CMP (Chip Multiprocessors and cache coherency), Core Multi-Threading, LL and SC instructions, etc.
http://classes.usc.edu/term-20191/classes/ee-457