EE354L: Introduction to Digital Circuits

Course Number & Title: **EE354L: Introduction to Digital Circuits**

Units: 4

Semester and time: Spring 2019 semester
http://classes.usc.edu/term-20191/classes/ee-354
Lecture: MW 10:00-11:50 AM in RTH105
Lecture: MW 2:00- 3:50 PM in RTH105
Labs: 4 labs each lab 2H 50M in OHE336
(i) 6:00-8:50 PM Mon. (ii) 5:00-7:50 PM Tues. (iii) 5:00-7:50 PM Wed. (iv) 6:00-8:50 PM Thurs.

Location: Lectures: RTH105; Labs in OHE336

Instructor: Gandhi Puvvada

Office: EEB 238

Office hours: 4 hours per week (4:10-6:00PM Monday; 2:30-4:30 PM Tuesday) in EEB 238 / EEB 203
http://www-classes.usc.edu/engr/ee-s/457/Gandhi_Office_Hours/Gandhi_Office_Hours_Sp2019.pdf

Contact information: gandhi@usc.edu, Office: (213) 740-4461, Cell: (310) 733-8025

Catalog Description:
http://catalogue.usc.edu/index.php

EE 354L Introduction to Digital Circuits (4, FaSpSm) Digital system design and implementation; synchronous design of datapath and control; schematic/Verilog-based design, simulation, and implementation in Field Programmable Gate Arrays; timing analysis; semester-end project. *Prerequisite:* EE 101 or EE 209. (Duplicates credit in EE 254.)

Learning objectives:

Upon completion of this course students will be able to:
1. Design, simulate, and build (implement on a FPGA board) a substantial digital system
2. Design a digital system using Verilog HDL (Hardware Description Language)
3. Understand RTL design (DPU and CU) and Timing design
4. Understand the use of an embedded processor in a digital system design
5. Compare dedicated hardware implementation with a processor-based implementation
6. Understand 8-bit processor pinout, address decoding and SRAM memory interface
7. Understand issues with Clock domain crossing, 4-way and 2-way handshake, single-clock and two-clock FIFOs (First-In First-Out buffers) and their application
8. Understand tristate buffers, open-drain devices, buses, bus arbiters, rotating prioritizer
9. Understand how serial busses work, and get to know I2C bus operational details
10. Finally design and implement a semester-end project

Website: https://blackboard.usc.edu/

TAs:
EE354L Head TA -- Yueh-Hsun Lin <yuehhsul@usc.edu>,
EE354L TA -- Jinglei Cheng <chen520@usc.edu>,
EE354L TA -- Kiran Nagendra <knagendr@usc.edu>,
EE354L TA -- Arun Sai Mamidala <mamidala@usc.edu>
Lab Mentor:
EE354L Mentor -- Ana Rescala <rescala@usc.edu>

Grader: EE354L Grader -- Akshay Keshavamurthy <keshavam@usc.edu>

Office hours: 1. Gandhi 4:10-6:00 PM Monday; 2:30-4:30 PM Tuesday Gandhi_Office_Hours_Sp2019.pdf
2. TAs' Hours: TBA
3. Grader Akshay: 12:30 – 1:30 Tu, Wed. in PHE330 (Hours observed simultaneously on BlueJeans)
Meeting ID: 7273838739 web link: https://uscviterbi.bluejeans.com/7273838739

Prerequisite: EE109 or EE209
Recommended Preparation: Basic programming skills taught in courses like EE109L (Introduction to Embedded Systems)

Optional Textbook: Digital Design: Principles and Practices, 4/E By John F. Wakerly
http://www.ddpp.com/
Required class-notes and lab manual: Class-notes and Lab Manual distributed online progressively

Recommended Reading: Readings will be posted on Blackboard or communicated via emails

Course Material: Class-notes and Lab Manual

EE354L is an intensive design course, reinforcing class-room lectures with homework and lab assignments.
Textbooks often fail to cover the design process adequately. The lecture material and the lab assignments were developed over the last 30 years of teaching this subject.

Attendance policy: http://www-classes.usc.edu/engr/ee-s/254/ee354l_attendance.html

Grading Policy (approximate weights) (approximately 47% in assignments and 53% in exams)**:**
Weights vary slightly from semester to semester. Example: Fall 2018 Grade sheet
Also, I use two scales (weights) for the three exams to compute the exam total and take the higher of the two for each student, so that if one does poorly in the Quiz+Midterm, he/she can try to do better in the final.

	Weight 1	Weight 2
HW	6.25	6.25
Short Exercises	2.75	2.75
LAB	25.00	25.00
Project	10.00	10.00
TA	3.00	3.00
Quiz	7.50	9.50
MT	17.50	20.50
Final	28.00	23.00
	100.00	100.00

Class Tentative Schedule: Topics and the order of lectures may change.
Listed below are the dates for the lecture and the lab.
http://classes.usc.edu/term-20191/classes/ee-354

We have four lab sessions every week. The detailed lab schedule is posted at
http://www-classes.usc.edu/engr/ee-s/254/ee254l_lab_manual/EE254L_Lab_Plan.pdf
MTWT (in the lab rows below) stands for Monday, Tuesday, Wednesday, and the Thursday and refers to the four labs every week.

Lec/Lab	Date	Day	Topics and Assignments
	January		
Lec#1	7	Mon	Course intro., DPU & CU (Data Path Unit and Control Unit), One-hot state assignment for CU design pdf .wmv , Mealy machine example -- Divider Design pdf .avi ,
Lec#2	9	Wed	State diagram Design examples .pdf .avi Detour lab pdf HW#5 Example of One-hot state assignment for CU design pdf dir
Lab#1		MTWT	Lab introduction pdf, Tools installation pdf (ISE for Synthesis, Modelsim for Simulation, etc.) , VDI
Lec#3	14	Mon	Data registers -- clocking and controlling pdf .avi ; Loop Counter Incrementation and Terminal Value Checking pdf .avi pdf pdf pdf ; ME (Mutually Exclusive) and AI (All Inclusive) rules in designing a state diagram pdf pdf .avi ; Intercept and Inject method of Data path Design using Synchronous Counter as an example pdf .avi ;
Lec#4	16	Wed	Verilog HDL Introduction pdf .avi , behavioral modeling pdf .avi Verilog HDL Data types pdf .avi and Sequential Statements pdf .avi
Lab#2		MTWT	Nexys-3 (FPGA Board) Intro. Time-Division multiplexed 7-segment Common Anode Display pdf pdf .avi Detour Signal State Machine (Schematic) pdf .avi
Lec#3	21	Mon	MLK Holiday
Lec#6	23	Wed	Verilog Blocking and Non-blocking assignments, .pdf .avi RTL coding in Verilog .pdf .avi .pdf .zip
Lab#3		MTWT	Verilog Introduction Labs (Synchronous and Asynchronous FF resets, and Divider RTL design in Verilog example design, Divider Moore machine design) .pdf .pdf .avi .pdf .zip
Lec#7	28	Mon	HW#8A first 6 pages of .pdf Q#2 Make A close to B pdf .wmv ; largest number divisible by 7 pdf wmv ; Copying two parts of a sorted array (finish 3.2 first and then work on 3.1) pdf wmv
Lec#8	30	Wed	Lab #6a RTL Coding -- Divider Example -- Debouncing, Single-stepping, and output coding pdf & .avi
	February		
Lab#4		MTWT	Number Lock State Machine, Nexys-3 Top design, all in Verilog .dir pdf

Lec#9	4	Mon	**Picoblaze** The following is a quick introduction to the topics below as a prelude to introducing PicoBlaze in the next lecture. Introduction to Memories, Processors, Processor pinout, Processor Address Map, Byte Addressability, Processor address decoding, I/O addresses, I/O ports, Input port may or may not require a storage register to hold input data before collection by the processor, Output port needs a storage register to hold the output data sent by the processor for display or transmission, Interrupts, Interrupt service routine, sharing a single interrupt request (INTR) pin and identifying the requester. PicoBlaze is not for data crunching, it is meant to provide control sequences to perform a job such as UART, etc.
Lec#10	6	Wed	Picoblaze introduction, Picoblaze Assembly Language, dir pdf pdf pdf 1.mp4 2.mp4
Lab#5		MTWT	Lab #6a RTL Coding -- Divider Example -- Debouncing, Single-stepping, and output coding pdf & .avi
Lec#11	11	Mon	Data-path design (a) small system design .pdf .avi BCD to Binary and reverse conversion Chapter 7 , Inches to Yards-Feet-Inches conversion pdf .avi, GCD design pdf .avi
Lec#12	13	Wed	Quiz preparation
Lab#6		MTWT	GCD (Greatest Common Divisor) design .pdf
Lec#13	18	Mon	Presidents' Day, university holiday
Lec#14	20	Wed	Picoblaze interface to external hardware, input and output ports, Hex Keypad .pdf .pdf .pdf
Lab#7		MTWT	Picoblaze introduction, EE354L_Get_acquainted_with_PicoBlaze.pdf .pdf
	22	Fri	**Quiz Exam: 8:00AM - 9:50 AM Please let me know if you have serious time conflict.**
Lec#15	25	Mon	Array processing in RTL, pointers and pointer incrementation, HW#8A .pdf Due dates and info: .pdf Directory .dir
Lec#16	27	Wed	Picoblaze Interrupts
	March		
Lab#8		MTWT	Keypad interface to Picoblaze .pdf , Demo: Divider on Pico .zip
Lec#17	4	Mon	Timing Design part 1 setup and hold margins, synchronizing asynchronous inputs .pdf HW#8 on Data Path Unit Design .pdf .wmv.zip
Lec#18	6	Wed	Timing Design part 2 reset synchronization, Shannon's expansion theorem applications .pdf Midterm review, Q#2, Q#3 from Sp2013 .pdf
Lab#9		MTWT	Writing Testbenches .dir .pdf
	11	Mon	March 10-17 Spring recess
	12	Wed	March 10-17 Spring recess
			March 10-17 Spring recess
Lec#19	18	Mon	Tristate Buffers, muxes and tristate buffers in Data-path design Q#2 MT_Sp12.pdf MT_ Sp12_sol.pdf
Lec#20	20	Wed	Decade counter pdf .zip Verilog HDL Blocking and Non-blocking assignments Last two pages pdf .avi Verilog Exam questions review .pdf P1.avi P2.avi
Lab #10		MTWT	Picoblaze Interrupts (i) using polling (ii) with no polling .pdf
Lec#21	25	Mon	Slack (make up), Midterm Review
Lec#22	27	Wed	Preparation for the midterm
Lab #11		MTWT	Timing Analysis and Timing Constraints .pdf Prepare for the semester end project: PMODs, VGA demo, LCD demo, File I/O demo, Logic Analyzer Demo, ChipScope Demo, Final Project proposals

	29	Fri	**Midterm Exam: 8:00AM - 10:50 AM Please let me know if you have serious time conflict.**
	April		
Lec#23	1	Mon	Chapter 11 Memories .pdf .wmv
Lec#24	3	Wed	Memories lecture completion and FIFO lecture introduction, FIFOs .pdf .wmv
Lab #12		MTWT	Final Project proposals approvals, Final Project Week 1
Lec#25	8	Mon	FIFO completion, Gray code, Binary<->Gray conversion, .pdf , Handshake .pdf .pdf
Lec#26	10	Wed	Epp protocol, and File I/O between PC and the FPGA using Epp protocol pages 10, 11, 12 of .pdf
Lab #13		MTWT	Final Project Week 2
Lec#27	15	Mon	File I/O completion
Lec#28	17	Wed	Ch 4_mux, Barrel shifters, priority encoders, Totem-pole and Open-collector output devices dir
Lab #14		MTWT	Final Project Week 3
Lec#27	22	Mon	UART Basics .pdf , I2C Bus Protocol .pdf
Lec#28	24	Wed	Special Counters Exam questions .pdf Review for the Final exam .pdf
Lab #15		MTWT	Final Project demonstration, presentation, and report submission
	May		
	2	Thurs day	**Final exam 7:30 AM – 10:30AM (Extended hours**, please let me know if you have conflict) http://classes.usc.edu/term-20191/finals/ Official slot is 8:00 AM to 10:00 AM. With your cooperation, I want to extend it to 7:30 AM to 10: AM Electrical Engineering 354 Thursday, May 2 8-10 a.m.

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Statement on Academic Conduct and Support Systems

Academic Conduct:

Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in *SCampus* in Part B, Section 11, "Behavior Violating University Standards" https://policy.usc.edu/scampus-part-b/. Other forms of academic dishonesty are equally unacceptable. See additional information in *SCampus* and university policies on scientific misconduct, http://policy.usc.edu/scientific-misconduct.

Support Systems:

Student Counseling Services (SCS) - (213) 740-7711 – 24/7 on call
Free and confidential mental health treatment for students, including short-term psychotherapy, group counseling, stress fitness workshops, and crisis intervention. https://engemannshc.usc.edu/counseling/

National Suicide Prevention Lifeline - 1-800-273-8255
Provides free and confidential emotional support to people in suicidal crisis or emotional distress 24 hours a day, 7 days a week. http://www.suicidepreventionlifeline.org

Relationship and Sexual Violence Prevention Services (RSVP) - (213) 740-4900 - 24/7 on call
Free and confidential therapy services, workshops, and training for situations related to gender-based harm.
https://engemannshc.usc.edu/rsvp/

Title IX Preserving the civil rights of the campus community
http://titleix.usc.edu/ http://titleix.usc.edu/prohibited-conduct/ http://titleix.usc.edu/resources/

Office of Equity and Diversity (OED)/Title IX Compliance – (213) 740-5086
Works with faculty, staff, visitors, applicants, and students around issues of protected class. https://equity.usc.edu/

Bias Assessment Response and Support
Incidents of bias, hate crimes and microaggressions need to be reported allowing for appropriate investigation and response. https://studentaffairs.usc.edu/bias-assessment-response-support/

The Office of Disability Services and Programs
Provides certification for students with disabilities and helps arrange relevant accommodations. http://dsp.usc.edu

Student Support and Advocacy – (213) 821-4710
Assists students and families in resolving complex issues adversely affecting their success as a student EX: personal, financial, and academic. https://studentaffairs.usc.edu/ssa/

Diversity at USC
Information on events, programs and training, the Diversity Task Force (including representatives for each school), chronology, participation, and various resources for students. https://diversity.usc.edu/

USC Emergency Information

Provides safety and other updates, including ways in which instruction will be continued if an officially declared emergency makes travel to campus infeasible, http://emergency.usc.edu

USC Department of Public Safety – 213-740-4321 (UPC) and 323-442-1000 (HSC) for 24-hour emergency assistance or to report a crime.
Provides overall safety to USC community. http://dps.usc.edu