University of Southern California

Ming Hsieh Department of Electrical Engineering

Course Number & Title: EE 536a, Mixed Signal Integrated Circuit Design

Units: 4

Semester: Fall 2018

Schedule: Mondays & Wednesdays 10:00 am – 11:50 am
Fridays: 12:00 – 12:50 pm

Location: OHE 120 (MW), OHE 100B (F)

Instructor: Hossein Hashemi

Office: PHE 616

Office Hours: Mondays & Wednesdays 9:00 am – 9:45 am

Contact Information: hosseinh@usc.edu, 213-740-3596

Teaching Assistant: Samer Idres (idres@usc.edu) TBD in PHE 530

Catalogue Description:

MOSFET operation and models; elementary amplifier configurations; biasing and references; frequency response; noise; feedback; operational amplifiers; frequency compensation; nonlinearity and mismatch; passive and active filters

Course Description:

EE 536a covers theory, analysis, and design of analog integrated circuits at the transistor level. The course includes a few design projects as homework assignments and a comprehensive final design project using state-of-the-art semiconductor technologies and computer aided design environments. The principles covered in this course enables designing low noise, high frequency, low power, analog integrated circuits such as operational amplifier and active filters.

Learning Objectives:

EE 536a is designed as the first graduate course covering theory, analysis, and design of analog integrated circuits. At the completion of the subject students will be able to analyze and design analog integrated circuits for wide range of applications such as wireless and wired

communications, biomedical implants, controls, computation, sensing, imaging, etc. The course serves as the pre-requisite for EE 536b covering basics and advanced mixed-signal integrated circuits.

Prerequisite: EE 479 or EE 448L

Main Text Book: B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw Hill, 2nd Edition, 2017.

Supplementary Texts:

- P. Grey, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Integrated Circuits*, John Wiley and Sons, 5th Edition, 2009.
- A. Sedra and K. Smith, *Microelectronic Circuits*, Oxford University Press, 6th Edition, 2009.
- D. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley and Sons, 1st Edition, 1997.

Readings: All lecture notes will be available on Blackboard.

Grading:

Homework (12)	10%
Midterm Exam	30%
Final Exam	40%
Design Projects	20%

Tentative Weekly Schedule

Week	Date	Subject	Readings	HW
1	Mon 08/20/2017	Review of basic MOSFET physics and models	Chapters 1, 2, 16, 17	HW 1 Assign
	Wed 08/22/2017	Review of basic MOSFET physics and models		
	Fri 08/24/2017	Review of single-stage amplifiers		
2	Mon 08/27/2017	Review of single-stage amplifiers	Chapter 3	HW 2 Assign
	Wed 08/29/2017	Single- and multi-stage amplifier examples		HW 1 Due
	Fri 08/31/2017	Single- and multi-stage amplifier examples		
3	Mon 09/03/2017	LABOR DAY	Chapter 4	HW 3 Assign
	Wed 09/05/2017	Differential amplifiers		HW 2 Due
	Fri 09/07/2017	Differential amplifiers		
4	Mon 09/10/2017	Differential amplifiers	Chapter 5	HW 4 Assign
	Wed 09/12/2017	Current mirrors, folded cascode, current amplification		HW 3 Due
	Fri 09/14/2017	Current mirrors, folded cascode, current amplification		
5	Mon 09/17/2017	Review of time- and frequency-domain analysis	Chapters 5, 6	HW 5 Assign
	Wed 09/19/2017	Frequency response		HW 4 Due
	Fri 09/21/2017	Frequency response		
6	Mon 09/24/2017	Frequency response	Chapter 6	HW 6 Assign
	Wed 09/26/2017	Frequency response (Miller theorem, zero calculation)		HW 5 Due
	Fri 09/28/2017	Frequency response (differential circuits)		
7	Mon 10/01/2017	Time constant analysis; bandwidth calculations	Chapter 6	HW 7 Assign
	Wed 10/03/2017	Mid-term exam		HW 6 Due
	Fri 10/05/2017	Noise		
8	Mon 10/08/2017	Noise	Chapter 7	HW 8 Assign
	Wed 10/10/2017	Noise		HW 7 Due
	Fri 10/12/2017	Noise		
9	Mon 10/15/2017	Feedback	Chapter 8, Lecture Notes	HW 8 Assign
	Wed 10/17/2017	Feedback		HW 7 Due
	Fri 10/19/2017	Feedback		
10	Mon 10/22/2017	Feedback	Chapter 8, Lecture Notes	HW 8 Assign
	Wed 10/24/2017	Feedback		HW 7 Due
	Fri 10/26/2017	Feedback		
11	Mon 10/29/2017	Feedback: stability	Chapter 10	HW 9 Assign
	Wed 10/31/2017	Feedback: stability		HW 8 Due
	Fri 11/02/2017	Feedback: stability		
12	Mon 11/05/2017	OTA: Single-stage single-ended & fully-differential	Chapter 9	HW 10 Assign
	Wed 11/07/2017	OTA Design		HW 9 Due
	Fri 11/09/2017	Common-mode feedback		
13	Mon 11/12/2017	OTA: Telescopic cascode + CMFB + compensation	Chapters 10	HW 11 Assign
	Wed 11/14/2017	OTA: Folded cascode + CMFB + compensation		HW 10 Due
	Fri 11/16/2017	Rail-rail OTA design		
14	Mon 11/19/2017	Biasing & references	Chapter 12	HW 12 Assign
	Wed 11/21/2017	Thanksgiving		HW 11 Due
	Fri 11/23/2017	Thanksgiving		
15	Mon 11/26/2017	OTA: Two-stage + compensation	Chapter 14	
	Wed 11/28/2017	Slew rate, Nonlinearity & Mismatch		HW 12 Due
	Fri 11/30/2015	Final project presentations		

Homework

Unless otherwise stated, homework assignments are due on Wednesdays at the beginning of the class. Solutions will be posted on the class website on the same day.

Late homework will not be accepted. No exceptions except institution-established emergency reasons; credit for such late homework is with the discretion of the professor.

Limited collaboration in solving homework problems is allowed. This includes reviewing and discussing the problems with current EE 536a students and TA prior to writing down your solution. Everybody has to write his/her own solution independently and make sure to fully understand it. Exchanging solutions, consulting with people other than class members, finding solutions on the web or elsewhere, etc. are not allowed. Violations result in losing the credit for the entire homework set in addition to a significant percentage of the overall course grade, all with the discretion of the professor.

All answers should be clearly and fully justified. If we can't figure out your steps from is turned in, points will be deducted, even if your final answer is correct.

One or more of the homework assignments include design problems as well as the typical analysis problems. Simulation and performance verification of the design problems will be in the Cadence environment.

Final Design Project

The final project will consist of a transistor-level design, analysis, and simulation of a complete integrated circuit such as a high-performance Operational Trans-conductance Amplifier (OTA) in the Cadence environment using a state-of-the-art semiconductor foundry process design kit. Design project must be completed individually. Final project grading will be based on design creativity, achieved specifications, completeness of the written report including comparison between analysis and simulation results, and the quality of the oral presentation including answering to the questions posed by the instructor and other classmates. The approximate timeline for the project is as follows:

Late October:	Announcement of the final project description
Last Monday of the class:	Due date for electronic submission of the project schematic
Last Friday of the class:	Oral presentations, and due date for submission of the report

Statement on Academic Conduct and Support Systems

Academic Conduct

Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in *SCampus* in Section 11, *Behavior Violating University Standards*https://scampus.usc.edu/1100-behavior-violating-university-standards-and-appropriate-sanctions/. Other forms of academic dishonesty are equally unacceptable. See additional information in *SCampus* and university policies on scientific misconduct, http://policy.usc.edu/scientific-misconduct/.

Discrimination, sexual assault, and harassment are not tolerated by the university. You are encouraged to report any incidents to the *Office of Equity and Diversity* http://equity.usc.edu/ or to the *Department of Public Safety* http://capsnet.usc.edu/department/department-public-safety/online-forms/contact-us. This is important for the safety whole USC community. Another member of the university community – such as a friend, classmate, advisor, or faculty member – can help initiate the report, or can initiate the report on behalf of another person. *The Center for Women and Men* http://www.usc.edu/student-affairs/cwm/ provides 24/7 confidential support, and the sexual assault resource center webpage sarc@usc.edu describes reporting options and other resources.

Support Systems

A number of USC's schools provide support for students who need help with scholarly writing. Check with your advisor or program staff to find out more. Students whose primary language is not English should check with the *American Language Institute* http://dornsife.usc.edu/ali, which sponsors courses and workshops specifically for international graduate students. *The Office of Disability Services and Programs* http://sait.usc.edu/academicsupport/centerprograms/dsp/home_index.htmlprovides certification for students with disabilities and helps arrange the relevant accommodations. If an officially declared emergency makes travel to campus infeasible, *USC Emergency Information* *http://emergency.usc.edu/*will provide safety and other updates, including ways in which instruction will be continued by means of blackboard, teleconferencing, and other technology.