EE354L: Introduction to Digital Circuits

Course Number & Title: **EE354L: Introduction to Digital Circuits**

Units: 4

Semester and time: Spring 2016 semester
http://classes.usc.edu/term-20161/classes/ee-354
Lecture: MW 10:00-11:50AM in SLH100
Labs: 3 labs each lab 2H 50M in OHE336
(i) 5:00-7:50 PM Tues. (ii) 5:00-7:50PM Wed. (iii) 6:00-8:50 PM Thurs.

Location: Lecture: SLH 100; Lab in OHE336

Instructor: Gandhi Puvvada

Office: EEB 238

Office hours: 4.5 hours per week and additional hours by appointment
http://www-classes.usc.edu/engr/ee-s/457/Gandhi_Office_Hours/Gandhi_Office_Hours_Sp2016.pdf

Contact information: gandhi@usc.edu, Office: (213) 740-4461, Home: (310) 839-3933
http://ee.usc.edu/faculty_staff/faculty_directory/puvvada.htm

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Catalog Description:

(Essentially same as the previous EE254L catalogue description: http://catalogue.usc.edu/schools/engineering/electrical/courses/)

EE 354L Introduction to Digital Circuits (4, FaSpSm) Digital system design and implementation; synchronous design of datapath and control; schematic/Verilog-based design, simulation, and implementation in Field Programmable Gate Arrays; timing analysis; semester-end project. *Prerequisite:* EE 101 or EE 154. (Duplicates credit in former EE 201/254L.)

Learning objectives:

Upon completion of this course students will be able to:
1. Design, simulate, and build (implement on a FPGA board) a substantial digital system
2. Design a digital system using Verilog HDL (Hardware Description Language)
3. Understand RTL design (DPU and CU) and Timing design
4. Understand Memories and FIFOs (First-In First-Out buffers) and their application
5. Understand tristate buffers, open-drain devices, barrel shifters, rotating prioritizers, and their applications
6. Understand how to interface I/O devices such as UART, VGA, LCDs, SSDs
7. Understand Bus protocols, bus arbiters, and handshake
8. Finally design and implement a semester-end project

Website: https://blackboard.usc.edu/

TAs:
1. EE354L TA -- Shreyas Girish Singapura singapur@usc.edu ,
2. EE354L TA -- Gunjae Koo gunjaeko@usc.edu,
3. EE354L TA -- Fangzhou Wang fangzhow@usc.edu

Grader: `EE354L Grader -- Prashanth Mahesh pmahesh@usc.edu`

Office hours: 1. Gandhi http://www-classes.usc.edu/engr/ee-s/457/Gandhi_Office_Hours/Gandhi_Office_Hours_Sp2016.pdf
2. TAs: TBA
3. Grader: Wednesdays from 12:00 noon to 1:30PM in PHE330

Prerequisite: EE 101 or EE209
Recommended Preparation: Basic programming skills taught in courses like EE109L (Introduction to Embedded Systems)

Optional Textbook: Digital Design: Principles and Practices, 4/E By John F. Wakerly
http://www.ddpp.com/
Required class-notes and lab manual: Class-notes and Lab Manual

Recommended Reading: Readings will be posted on Blackboard

Course Material: Class-notes and Lab Manual

EE354L is an intensive design course, reinforcing class-room lectures with homework and lab assignments.
Textbooks often fail to cover design adequately. The lecture material and the lab assignments were developed over the last 25 years of teaching this subject.

Grading Policy (approximate weights)**:**

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Homework:  10%
Labs:      30%
Project:   10%
TA:         5%
Quiz:       5%
Midterm:   20%
Final:     25%
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Class Tentative Schedule: Topics and the order of lectures may change.
Listed below are the dates for the lecture and the lab.
http://classes.usc.edu/term-20161/classes/ee-354

The detailed lab schedule is posted at
http://www-classes.usc.edu/engr/ee-s/254/ee254l_lab_manual/AdditionalStuff/EE354L_Lab_Plan.pdf

Lec/Lab	Date	Day	Topics and Assignments
	January		
Lec#1	11	Mon	Course intro., DPU & CU (Data Path Unit and Control Unit), One-hot state assignment for CU design pdf .wmv , Detour lab pdf
Lec#2	13	Wed	Nexys-3 (FPGA Board) Intro. Time-Division multiplexed 7-segment Common Anode Display pdf .avi
Lab#1		TWT	Lab introduction pdf, Tools installation pdf (ISE for Synthesis, Modelsim for Simulation, etc.)
Lec#3	18	Mon	MLK Holiday
Lec#4	20	Wed	ME (Mutually Exclusive) and AI (All Inclusive) rules in designing a state diagram pdf .avi HW#1 (EE101/EE209 review) pdf, HW#5 Example of One-hot state assignment for CU design pdf dir
Lab#2		TWT	Detour Signal State Machine (Schematic) pdf .avi
Lec#5	25	Mon	Mealy machine example -- Divider Design pdf .avi , Data registers -- clocking and controlling pdf .avi
Lec#6	27	Wed	Loop Counter Incrementation and Terminal Value Checking pdf .avi , State diagram Design examples .pdf .avi
Lab#3		TWT	Number Lock State Machine using one-hot state assignment method (Schematic) pdf
	February		
Lec#7	1	Mon	Verilog HDL Introduction pdf .avi , behavioral modeling pdf .avi
Lec#8	3	Wed	Verilog HDL Data types pdf .avi and Sequential Statements pdf .avi
Lab#4		TWT	Verilog Introduction Labs (Arbitrary clock divider, Weighted coin and die simulator, Synchronous and Asynchronous FF resets, and Divider RTL design in Verilog) .pdf /.zip on Bb
Lec#9	8	Mon	Lab #6a RTL Coding -- Divider Example -- Debouncing, Single-stepping, and output coding pdf & .avi
Lec#10	10	Wed	Exam Questions on Verilog pdf P1.avi P2.avi
Lab#5		TWT	State Machine Design using Verilog HDL- Number Lock State Machine pdf Top Design using Verilog HDL - Number Lock State Machine
Lec#11	15	Mon	Presidents' Day, university holiday
Lec#12	17	Wed	Data-path design (a) small system design .pdf .avi BCD to Binary and reverse conversion Chapter 7 , Inches to Yards-Feet-Inches conversion pdf .avi, GCD design pdf .avi
Lab#6		TWT	Lab #6a RTL Coding -- Divider Example -- Debouncing, Single-stepping, and output coding pdf & .avi
Lec#13	22	Mon	Decade counter pdf .zip Verilog HDL Blocking and Non-blocking assignments Last two pages pdf .avi Verilog Exam questions review .pdf P1.avi P2.avi
Lec#14	24	Wed	**Quiz Exam 10:00AM -11:50AM (No extended hours)**
Lab#7		TWT	GCD (Greatest Common Divisor) design .pdf
Lec#15	29	Mon	HW#8A .pdf Q#2 .pdf .wmv Q#1 .pdf .wmv
	March		

Lec#16	2	Wed	Microprogrammed Control Unit .pdf .avi
Lab#8		TWT	Slack – to make up/catch up
Lec#17	7	Mon	uPCU Questions from previous exams .pdf P1.avi P2.avi
Lec#18	9	Wed	HW#6 on uPCU Introduction .pdf .avi
Lab#9		TWT	Writing Testbenches .pdf
	14	Mon	March 14-20 Spring recess
	16	Wed	March 14-20 Spring recess
			March 14-20 Spring recess
Lec#19	21	Mon	Tristate Buffers, muxes and tristate buffers in Data-path design Q#2 MT_Sp12.pdf MT_ Sp12_sol.pdf
Lec#20	23	Wed	Timing Design part 1 setup and hold margins, synchronizing asynchronous inputs .pdf HW#8 on Data Path Unit Design .pdf .wmv.zip
Lab #10		TWT	Microprogrammed control unit – Merging two arrays .pdf
Lec#21	28	Mon	Timing Design part 2 reset synchronization, Shannon's expansion theorem applications .pdf Midterm review, Q#2, Q#3 from Sp2013 .pdf
Lec#22	30	Wed	**Midterm Exam: Two choices: (i) 9:00AM -11:50AM (ii) 10:00AM - 12:50PM Extended hours**
Lab #11		TWT	Prepare for the semester end project: PMODs, VGA demo, LCD demo, File I/O demo, Logic Analyzer Demo, ChipScope Demo, Final Project proposals
	April		
Lec#23	4	Mon	Chapter 10 Counters .pdf .avi Special Counters Exam questions .pdf
Lec#24	6	Wed	Slack (make up)
Lab #12		TWT	Timing Analysis and Timing Constraints .pdf Final Project proposals approvals
Lec#25	11	Mon	Chapter 11 Memories .pdf .wmv
Lec#26	13	Wed	Memories lecture completion and FIFO lecture introduction, FIFOs .pdf .wmv
Lab #13		TWT	Final Project
Lec#27	18	Mon	FIFO completion, Gray code, Binary<->Gray conversion, .pdf
Lec#28	20	Wed	Ch 4_mux, Barrel shifters, priority encoders, Totem-pole and Open-collector output devices dir
Lab #14		TWT	Final Project
Lec#27	25	Mon	UART Basics .pdf , I2C Bus Protocol .pdf
Lec#28	27	Wed	Review for the Final exam .pdf
Lab #14	2	TWT	Final Project demonstration, presentation, and report submission
	May		
	9	Mon	**Final exam 7:30 AM – 10:30AM (Extended hours, please let me know if you have conflict)**
			http://classes.usc.edu/term-20161/finals/

Statement on Academic Conduct and Support Systems

Academic Conduct

Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in *SCampus* in Section 11, *Behavior Violating University Standards* https://scampus.usc.edu/1100-behavior-violating-university-standards-and-appropriate-sanctions. Other forms of academic dishonesty are equally unacceptable. See additional information in *SCampus* and university policies on scientific misconduct, http://policy.usc.edu/scientific-misconduct.

Discrimination, sexual assault, and harassment are not tolerated by the university. You are encouraged to report any incidents to the *Office of Equity and Diversity* http://equity.usc.edu or to the *Department of Public Safety* http://capsnet.usc.edu/department/department-public-safety/online-forms/contact-us. This is important for the safety of the whole USC community. Another member of the university community – such as a friend, classmate, advisor, or faculty member – can help initiate the report, or can initiate the report on behalf of another person. *The Center for Women and Men* http://www.usc.edu/student-affairs/cwm/ provides 24/7 confidential support, and the sexual assault resource center webpage http://sarc.usc.edu describes reporting options and other resources.

Support Systems

A number of USC's schools provide support for students who need help with scholarly writing. Check with your advisor or program staff to find out more. Students whose primary language is not English should check with the *American Language Institute* http://dornsife.usc.edu/ali, which sponsors courses and workshops specifically for international graduate students. *The Office of Disability Services and Programs* http://sait.usc.edu/academicsupport/centerprograms/dsp/home_index.html provides certification for students with disabilities and helps arrange the relevant accommodations. If an officially declared emergency makes travel to campus infeasible, *USC Emergency Information* *http://emergency.usc.edu* will provide safety and other updates, including ways in which instruction will be continued by means of blackboard, teleconferencing, and other technology.