USC Viterbi School of Engineering

Revised syllabus showing new Quiz and MT dates on Thursdays

EE 457 Computer Systems Organization
Units: 4
Spring 2016 – Mon. Wed. 4:00-5:50PM in GFS118
Tues. Thurs. 5:00-6:50PM in OHE136
Location: GFS118 & OHE136

Instructor: Gandhi Puvvada
Office: EEB 238
Office Hours: 2:00-3:30PM MW, 3:00-4:30PM T in EEB 238
Contact Info: gandhi@usc.edu,
Office phone: (213) 740-4461,
Home phone: (310) 839-3933

Teaching Assistants: **Jizhe Zhang** and **Pezhman Mamdouh**
Mentors: **Bo Zhang** and **Kalpana Singla**
Office: PHE330 **Office Hours: click here**
Contact Info: jizhezha@usc.edu mamdouh@usc.edu
zhan254@usc.edu ksingla@usc.edu

Special registration requirements for EE457 in Spring 2016

The EE457 course is changing from 3 units to 4 units and the contact hours are changing from 1H 20M twice a week to 1H 50M twice a week. In Spring 2016 (the transitional semester) all students registered in EE 457 must also register in one unit of accompanying Directed Research (DR) - EE 490 for undergraduates and EE 590 for graduate students. To register for 1-unit DR, please login to myviterbi.usc.edu using your USC net login ID and password, and fill-up the form as shown below. Prof. Puvvada will approve your DR application and the EE Department will provide you a D clearance. Then you can register for the 1-unit DR.

	Undergraduate students	**Graduate students**
Select Term	Spring 2016	Spring 2016
Select Class	EE 490 (Undergraduates only)	EE 590 (Masters level)
Select Units	1	1
Select Faculty	Puvvada, Gandhi	Puvvada, Gandhi
Project Description	EE457 additional unit	EE457 additional unit

Undergraduate students shall register for 1 unit of **EE490** and they will receive the same **letter grade** for this 1 unit DR that they receive for the 3-unit EE457 at the end of Spring 2016.

Graduate students shall register for 1 unit of **EE590**. Unlike the undergraduates, they do not receive a letter grade for this 1 unit. They will receive a Credit/No-Credit (**CR/NC**) grade at the end of Spring 2016. If they get a C grade or above in the 3-unit EE457, they get credit (**CR** grade) for the 1-unit EE590. If they get a C- grade or below in the 3-unit EE457, then they get no credit (**NC** grade) for the 1-unit EE590.

1. Course Description

This course covers computer organization and design. It provides CS/CE/EE students a substantial understanding of a CPU at its logic design level. Design of the control unit and the data path unit of a simple multi-clock-cycle CPU and a pipelined CPU is covered in detail. Hardware support for exceptions, dynamic scheduling of instructions (Tomasulo algorithm to execute instructions in an out-of-order fashion), and branch prediction are also discussed. Computer arithmetic and memory hierarchies (cache, main memory, virtual memory) are also covered. Students design in Verilog and use ModelSim simulator to verify their RTL design/simulation exercises.

2. Learning Objectives

At the end of the course, students are expected to feel confident to perform logic design of a CPU or any hardware system utilizing pipelining and other RTL techniques and proceed to graduate courses in computer architecture or general hardware design. This course also expected to improve students' design skills and analytical skill.

3. Course administration

a) Course prerequisites: EE354L (previously EE254L or EE201L) Introduction to Digital Circuits is a *necessary* prerequisite. Undergraduate students without this prerequisite will not be able to do this course. Graduate students are expected to have taken a logic design course and a course covering some assembly language in their undergraduate course work before taking this course.

Recommended Preparation: Familiarity with the following items at an introductory level is expected.

1. Programming in an assembly language of any processor (CISC or RISC)
2. Digital Logic design at RTL level (Register Transfer Language Level)
3. Design entry using Verilog HDL (Hardware Description Language) and simulation

b) Classes: http://classes.usc.edu/term-20161/classes/ee-457

Discussion class is *not optional*. The homeworks and the lab assignments are primarily discussed during the discussion class. Important additional material may be covered in the discussion class.

c) Examinations: No makeup exams.

Please note that EE457 exams are long (2H 50 minutes) as they are design exams. I do not want to hurry you up.

One quiz (~10%), one midterm (~20%), and the final exam (~30%)

The "Quiz" slot (Qz **TBA** ~~10:00 – 11:50 AM Friday~~))
We will utilize this slot only twice in the whole semester to conduct a quiz and a midterm exam.
So it is OK to have schedule conflict with the quiz slot provided you agree to make yourself available for these two occasions.

Quiz (~10%): Thursday Feb. 11, 2016 ~~Friday Feb. 12, 2016~~ 05:00 PM - 07:50 PM PST
Midterm (~20%): Thursday Mar. 24, 2016 ~~Friday Mar. 25, 2016~~ 05:00 PM - 07:50 PM PST

April 8	Last day to drop a class with a mark of "W"

http://classes.usc.edu/term-20161/calendar/

Note: EE457 Final Exam is as per the Exceptions Schedule posted at the bottom of:
http://classes.usc.edu/term-20161/finals/
Final Exam (~30%): Saturday, May 7, 2016 10:30 AM - 1:30 PM PST (official slot of 11 a.m to 1 p.m. extended by 1 hour by starting 30 minutes early and ending 30 minutes late).

d) Grading Policy:

Course weights	Percentage	
Assignments		Late submission penalty for assignments
Homeworks	~7%	5% per day up to 3 days if solution is not given out
Labs	~ 28%	3% flat penalty up to 3 days
Class participation		
Short exercises	~ 5%	In-class exercises, short exercises posted on D2L, etc.
Exams		
Quiz	~ 10%	no make-up exam
Midterm	~ 20%	no make-up exam
Final	~ 30%	no make-up exam
Penalty for lecture absence: 1% for 3rd, 4th; 2% for 5th and after		
Penalty for discussion absence: 0.5% for 3rd, 4th; 1% for 5th and after		

e) Academic Accommodations:

Any student, requiring academic accommodations based on a disability, is required to register with the Center for Academic Support and Disability Services and Programs (CAS & DSP) each semester.
A letter of verification for approved accommodations can be obtained from CAS & DSP.
Please make sure that the letter is delivered to me as early in the semester as possible (no less than 2 weeks before an exam).
The CAS & DSP office is located in STU 301.
Their phone number is (213) 740-0776.
http://sait.usc.edu/academicsupport/centerprograms/dsp/home_index.html

f) Miscellaneous administrative matters:

Lecture class attendance, penalty for absence, and minimum required performance:

If you miss more than 2 lecture meetings, you will start noticing that you are falling behind.
If you miss more than 5 lecture meetings, you may as well drop the course.
It is a design course requiring continuity in your learning process. So please attend every lecture meeting.
The following penalty rules do not apply to remote students, as I cannot monitor their attendance. They are allowed to watch the lecture in the evening/late night.
Penalty for lecture absence: 1% for 3rd, 4th; 2% for 5th and after.
Penalty for discussion absence: 0.5% for 3rd, 4th; 1% for 5th and after.
http://www-classes.usc.edu/engr/ee-s/457/EE457_attendance_policy.html

Homeworks shall be done individually. Design and simulation labs can be performed either individually or in teams of two students (2 per team). But occasionally, design labs may be assigned as individual

assignments.
Teams shall submit one set of Verilog code and results online.
However justifications/explanations, state diagrams, and answers to questions at the end of the lab assignment (**paper submissions), shall be prepared individually.** *Copying is different from discussing ideas with other students.*
You are encouraged to share your thoughts on homework, design labs, and design lab reports with others as long as you act like a *Teaching Assistant* who tries to help without giving away the solution.
Absolutely no copying. Do NOT try to copy any assignment. We have ways to find if a design/simulation lab has been copied. Try not submitting a non-working lab as we give very little credit for a non-working lab.
We are here to help you and guide you in your debugging. If you submit a **non-working design/lab** and do not write on the top of it in **BIG** letters that it is NOT WORKING (and further do not inform the instructor, the TAs, and the lab graders through an email before submission), we will treat it as an attempt to cheat. This is very important.

Academic dishonesty cases will be dealt with severely. You must have gone through the short presentation on Academic Integrity at USC posted at
http://www.usc.edu/libraries/about/reference/tutorials/academic_integrity/
http://usclibraries.adobeconnect.com/academicintegrity

Another important resource is the Student Judicial Affairs and Community Standards (SJACS) website http://www.usc.edu/student-affairs/SJACS/index.html .
You may also want to visit
http://www.usc.edu/student-affairs/SJACS/pages/students/community_standards.html
University policy requires that all academic integrity violations are reported to Student Judicial Affairs and Community Standards (SJACS).

We will try to make the assignments due on times far from the class time.
This is to make sure that students do not miss classes to complete their assignments.

Please check your email regularly. Also visit the DEN D2L regularly at https://courses.uscden.net/
D2L stands for Desire2Learn, a Learning Management System used by DEN.
https://gapp.usc.edu/graduate-programs/den/technical-support/Desire2Learn

4. Design/simulation labs sequence:

Approximately one lab (or one part of one lab) will be assigned every week starting from the second week.

The labs make up **25%** to **30%** of your course credit.

0) Introduction to Verilog HDL entry and simulation in Modelsim

1) Max. Min. finder State Machine Design Lab #1 Part #1, Part #2, Part #3 (M1, M2, M3, M4)

2) Design of a 32-bit ALU Lab #3

3) Multi-cycle CPU Design Lab #4 Part #4 (only paper submission)

4) Design of a Pipelined CPU Lab #6 Part #4 and Part #5 (only paper submission)

5) FIFO and its application

6) Pipeline labs
Design of a 3-element adder Lab #7 Part #1, #2,
Design of a simple pipeline Lab 7 Part #3 (Sub parts SP1, SP2)
RTL Coding of a simple pipeline Lab 7 Part #3 (Sub parts SP3, SP3)

7) ROB and its application

Example Weights of the labs: Note that some labs have zero weights as you are not asked to submit these labs. However you are still responsible for reading the lab design and are able to answer questions on these items also on the exams. Labs and HWs vary slightly from semester to semester.

. LABS		
Lab #	nts	weight
1P1	100	0.50
1P2	100	0.70
1P3_M1	100	0.60
1P3_M2	100	0.60
1P3_M3	100	0.60
1P3_M4	100	0.60
1_Paper	100	0.60
FIFO_P1	100	0.60
FIFO_P2	100	1.20

J LABS		
Lab #	nts	weight
3	100	0.80
3_paper	100	0.60

J LABS		
Lab #	nts	weight
4P1	100	0.00
4P23	100	0.00
4P4	100	1.10
6P1	100	0.00
6P2P3	100	0.00
6P4	100	1.10
6P5	100	0.00
7P1	100	0.00
7P1&P2 Paper	100	1.20
P3_SP1&2 Paper	100	1.20
7P3_SP1	100	1.20
7P3_SP2	100	0.00
7P3_SP3	100	1.20
7P3_SP4	100	1.20
ROB_P2	100	1.30

5. Readings:

The required readings are class notes and sections of the textbook. Please make it a practice to read regularly. It is important to clarify any items that are not clear in that week itself. Students, who postpone reading, gradually drift away from the rest of the class and eventually perform very poorly on the exams and design/simulation labs.

Primary References:

Class Notes (required): Please buy from the university (USC) bookstore.
Remote students can place their orders online for the class notes and other items at the following (They may have to wait for a week to place their order):
USC Bookstores => Book Division => Distance Education
http://uscbookstore.com/courselistbuilder.aspx
If there is any problem, please call (213) 740-TEXT and also let me know if the problem cannot be resolved.

Lab Manual: We prefer to distribute the lab assignments progressively as pdf files. We can review and revise each assignment (if needed) and post it on the D2L.

Textbook/Verilog Guide:
1. Computer Organization & Design - The Hardware and Software Interface 5th edition
By D. A. Patterson (Berkeley) and J. L. Hennessey (Stanford)
You can buy it from the university (USC) bookstore or any place (such as online bookstores).
http://store.elsevier.com/Computer-Organization-and-Design/David-Patterson/isbn-9780124077263/
If you have the 4th edition, that is fine too.

2. The Verilog 2001 Reference Guide by Esperan (Cadence)
You need this for your Verilog-based design/simulation labs. **You can use it in the EE457 exams**.
Esperan (Cadence) does not sell it to individuals. They provided the pdf file to us free. It is posted on the BB. We will bring a few printed copies to the exam hall and you can borrow a copy for a short time.

Secondary References (Do not buy these):

1. EE101 and EE354L (EE254L) Textbook: Digital Design Principles and Practices By John F. Wakerly
2. EE557 Textbook: Parallel Computer Organization and Design by Dubois, Annavaram, and Stenstrom
3. Computer Architecture - A Quantitative Approach By D. A. Patterson and J. L. Hennessy

6. Course Schedule by week for Spring 2016:

Chapter numbers point to chapters in my class notes (http://www-classes.usc.edu/engr/ee-s/457/EE457_Classnotes/).
Homeworks and labs are due 1 week after they are assigned.

# of lectures	Lecture #	Item	Homework /Lab
2	1, 2 Week #1 1/11-1/15	**Ch#1** Intro to course, review of prerequisite material, Review data path and control unit design, Moore and Mealy, Glitches in control signals, Data registers with Data enable, State diagram design, All Inclusive and Mutually Exclusive rules,	HW#1
0		Verilog coding: Watch the 6-part EE354L lectures at home and learn by yourselves. Install Modelsim and learn to use the tool by yourself	Tools installation
1	3 Week #2 1/18-1/22	Compare and contrast: state diagram vs. flow-chart, Min-Max (a 6-part lab)	Lab #1
1	4 Week #2 1/18-1/22	**Ch#2** Performance, MIPs, MFLOPs	HW #2
2	5, 6, Week #3 1/25-1/29	**Ch#3** MIPs ISA, SLT, SLTU lw, sw, Byte addressable processors, memory addresses. also cover word addresses in a byte addressable processor	HW#1B
2	7, 8, Week #4 2/1-2/5	**Ch#4 P1** Review overflow detection in unsigned and signed arithmetic and ALU design	ALU lab Lab #3
2	9, 10, Week #5 2/8-2/12	**Ch#5 P1** Single Cycle CPU,	HW #5A (Singlei-cycle CPU)
0		**Quiz exam** on Thursday Feb. 11, 2016 5:00PM-7:50PM in HAR101	Quiz slot was TBA

2	11, 12 Week #6 2/15-2/19	**Ch#5 P2** multi-cycle CPU Datapath and control design **Ch#5 P2** Multi-cycle CPU 2nd edition design	Lab 4 Part #4 (Multi-cycle CPU) (paper submission) HW #5B (Multi-cycle CPU)
4	13,14, 15, 16 Week #7,8 2/22-3/4	**Ch#6** 5-stage pipeline: data dependency solutions (Compiler solution, HDU & FU), and branch implementations (late branch vs. early branch), branch delay slots. Also cover exceptions.	Pipelining Lab 6 – Part 4 (paper submission)
2	17, 18 Week #9 3/7-3/11	**Ch#7 P1** Cache: Mapping techniques, CPU address division into fields and connect address to Cache Data RAMs, Cache Tag RAMs,.	Cache HW #6 Pipeline lab #7 P1 and P2 paper
	Week #10 3/14-3/18	**Spring Recess**	
2	19, 20 Week #11 3/21-3/25	**Ch#7 P2** Virtual memory: Multi-level page table, PTBR, principle of inclusion. TLBs, and interleaved main memory	FIFO lab
0		**Midterm exam** on Thursday March 24, 2016 5:00PM-7:50PM in HAR101	Quiz slot was TBA
2	21, 22 Week #12 3/28-4/1	Virtual memory, Exceptions, Brach Prediction, 1-bit and 2-bit predictors, BPB, BTB	Virtual Memory HW #7
2	23, 24 Week #13 4/4-4/8	Out of order execution and Tomasulo Part 1 (IoI_OoE_OoC), WAR and WAW hazards in OoO execution, IFQ (Instruction prefetch queue), dispatch unit, issue queues, issue unit, CDB, ROB	Lab #7 P3 Sub Parts 1, 2 (paper submission)
2	25,26 Week #14 4/11-4/15	Tomasulo Part 2 (IoI_OoE_IoC), ROB, ROB search, Speculative execution and selective flushing if branch was mispredicted, exception handling,	ROB lab
2	27, 28 Week #15 4/18-4/22	**Ch#9** Parallel processing, semaphores, Read-Modify-Write (RMW) race, atomic operations on shared variables, CMP, Snoopy Cache Coherency protocols, Write through vs. write-back, MSI, MOESI	Pipeline RTL coding lab Lab #7 P3 Sub Parts 3, 4
1	29 Week #16 4/25-4/29	CMT, Thread-level parallelism, non-blocking cache, MPI	
1	30 Week #16 4/25-4/29	Locks, Atomic operations, LL and SC instructions in MIPs	
		Final exam on Saturday May 7, 2016 10:30AM – 1:30PM as stated in the exceptions list at the bottom of http://classes.usc.edu/term-20161/finals/ Electrical Engineering 457 Final Exam is comprehensive but focuses on later topics.	Final exam slot extended

Statement on Academic Conduct and Support Systems

Academic Conduct

Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in *SCampus* in Section 11, *Behavior Violating University Standards* https://scampus.usc.edu/1100-behavior-violating-university-standards-and-appropriate-sanctions/. Other forms of academic dishonesty are equally unacceptable. See additional information in *SCampus* and university policies on scientific misconduct, http://policy.usc.edu/scientific-misconduct/.

Discrimination, sexual assault, and harassment are not tolerated by the university. You are encouraged to report any incidents to the *Office of Equity and Diversity* http://equity.usc.edu/ or to the *Department of Public Safety* http://capsnet.usc.edu/department/department-public-safety/online-forms/contact-us. This is important for the safety whole USC community. Another member of the university community – such as a friend, classmate, advisor, or faculty member – can help initiate the report, or can initiate the report on behalf of another person. *The Center for Women and Men* http://www.usc.edu/student-affairs/cwm/ provides 24/7 confidential support, and the sexual assault resource center webpage sarc@usc.edu describes reporting options and other resources.

Support Systems

A number of USC's schools provide support for students who need help with scholarly writing. Check with your advisor or program staff to find out more. Students whose primary language is not English should check with the *American Language Institute* http://dornsife.usc.edu/ali, which sponsors courses and workshops specifically for international graduate students. *The Office of Disability Services and Programs* http://sait.usc.edu/academicsupport/centerprograms/dsp/home_index.htmlprovides certification for students with disabilities and helps arrange the relevant accommodations. If an officially declared emergency makes travel to campus infeasible, *USC Emergency Information http://emergency.usc.edu/*will provide safety and other updates, including ways in which instruction will be continued by means of blackboard, teleconferencing, and other technology.