EE599: Advanced Transistor Physics and Technology

Syllabus

Spring 2016

Course Description

In this course, students will learn the how's and why's of transistor device scaling and how it relates to logic circuit performance. This course will focus on giving students (i) the ability to look at the IEDM papers from Intel or TSMC and predict how the latest and greatest transistors will affect logic circuit design, and (ii) analyse new and upcoming transistor technologies to predict their potential for next generation circuits. We will also briefly look at understanding some of the physical sources of variability and how these process corners could affect MOSFET performance and failure.

In detail, this course will cover (i) basic MOSFET physics and models, (ii) modern day MOSFETs such as FinFETs, and (iii) what technologies could possibly come next. Students will be able to understand the challenges of scaling devices to the sub-10 nm node from both device physics and fabrication technology perspectives.

Suggested Prerequisite: EE537

Course Schedule

- Week 1 – A refresher on semiconductor basics
- Week 2 – Basic semiconductor devices – the PN junction and MS junction
- Week 3 – A high level introduction to MOSFET device physics, and how tradeoffs in MOSFET device design affects simple logic circuit performance
- Week 4 – Understanding the heart of a MOSFET- the MOS capacitor (part 1)
- Week 5 – Understanding the heart of a MOSFET- the MOS capacitor (part 2)
- Week 6 – Taking a deep dive into MOSFET device physics (part 1)
- Week 7 – Taking a deep dive into MOSFET device physics (part 2)
- Week 8 – Learning about the physics that make scaling devices difficult – short channel phenomena (part 1)
- Week 9 – Learning about the physics that make scaling devices difficult – short channel phenomena (part 2)
- Week 10 – Today's MOSFETs (part 1)
- Week 11 – Today's MOSFETs (part 2)
- Week 12 – Tomorrow's MOSFETs (part 1)
- Week 13 – Tomorrow's MOSFETs (part 2)
- Week 14 – Beyond MOSFETs – what are the technologies that could potentially replace standard CMOS (part 1)
- Week 15 – Beyond MOSFETs – what are the technologies that could potentially replace standard CMOS (part 2)

Prerequisite Knowledge

Students should have taken an undergraduate level device physics course, and have a basic knowledge of band diagrams, current transport mechanisms, metal-semiconductor junctions, pn junctions, MOS capacitors, and MOSFETs/BJTs.

Evaluation Criteria

Course grades will be based upon the following:

- Homework - 10%
- 2 Midterms - 50%
- Final - 40%

Reading Material

Recommended (but not required) texts:
Fundamentals of Modern VLSI Devices – Yuan Taur, Tak Ning
Physics of Semiconductor Devices – S. M. Sze, Kwok Ng

Statement for Students with Disabilities

Any student requesting academic accommodations based on a disability is required to register with Disability Services and Programs (DSP) each semester. A letter of verification for approved accommodations can be obtained from DSP. Please be sure the letter is delivered to me (or to TA) as early in the semester as possible. DSP is located in STU 301 and is open 8:30 a.m.–5:00 p.m., Monday through Friday. The phone number for DSP is (213) 740-0776.

Statement on Academic Integrity

USC seeks to maintain an optimal learning environment. General principles of academic honesty include the concept of respect for the intellectual property of others, the expectation that individual work will be submitted unless otherwise allowed by an instructor, and the obligations both to protect one's own academic work from misuse by others as well as to avoid using another's work as one's own. All students are expected to understand and abide by these principles. *Scampus*, the Student Guidebook, contains the Student Conduct Code in Section 11.00, while the recommended sanctions are located in Appendix A: http://www.usc.edu/dept/ publications/SCAMPUS/gov/.Students will be referred to the Office of Student Judicial Affairs and Community Standards for further review, should there be any suspicion of academic dishonesty. The Review process can be found at: http://www.usc.edu/student-affairs/SJACS/.