Spring 2016 Syllabus **EE 101** Gandhi Puvvada

Introduction to Digital Logic

Abstract:
This course introduces digital logic design basics which are fundamental to all computers and other digital hardware. Number systems, Boolean algebra, and analysis and design of combinational and sequential circuits are covered. Practical design techniques along with theory and principles will be taught. Functioning of the paper-pencil designs is confirmed via Verilog simulation. RTL design using Verilog is emphasized.

Instructor Info:

Instructor:	Gandhi Puvvada	Office Hours:	2:00-3:30PM MW, 3:00-4:30PM Tu
Office:	EEB 238		
E-mail:	gandhi@usc.edu	Office Phone:	(213) 740-4461

TA's and Grader Info:

TA:	Moises Herrerabuitrago	Grader:	Sushanth Bhushan
Office:	PHE320	Office:	PHE330
Office Hours:	See Blackboard	Office Hours:	See Blackboard
E-mail:	herrerab@usc.edu	E-mail:	sushantb@usc.edu

Course Materials and Info:

Online Content (Blackboard):	http://blackboard.usc.edu (use your USC NetID username and password)
Class Notes (Required):	Available at the Bookstore
References (**NOT** Required):	"Digital Design Principles and Practices" 4th Edition, by J.F. Wakerly (ISBN: 0131733494)

Grading Policy:

Participation and Homework	~10%
Labs	~20-30%
Quiz	~10-15%
Midterm	~20-25%
Final Exam	~30-40%

Homeworks: *Homeworks are your key to learning*. Only by doing problems on your own, you will develop the logic skills and understanding to perform well on exams. You are expected to *present your own work with your own creative solutions.* **Experience has shown that those students who put in the effort on these homeworks, struggled with problems, asking questions when they did not understand a problem, did the best in this course.**

Homeworks are is due at the **beginning** of the discussion class or lecture class. **Late homework will be accepted with a 5% deduction per day** for up to 2 days only if solution is not distributed. Late homework can be submitted by slipping under my office door except on the day of lecture/discussion. On the lecture/discussion days, late homework can be submitted at the beginning of the class. **Homework will not be accepted after solutions are posted or distributed**. Usually solutions are posted/distributed in 1 to 2 days after the due date. If you cannot make it to a lecture, turn it in early or have a friend turn it in. You will be expected to go through the listed sections of the lecture/discussion slides and class notes after every lecture/discussion before the next meeting (lecture or discussion).

Discussion/Lab: Discussion sections will be a mix of review/example problems and small lab exercises. Lab exercises will consist of design and simulation of combinational logic and sequential logic using Verilog HDL and Modelsim HDL simulation tool. Students will be required to submit their Verilog code and results text file to the UNIX class account using submit command on Unix.

Exams: All exams will be closed book. The Quiz and the Midterm exams will be taken in the Discussion section. There will be no calculators allowed, just bring a few pencils and an eraser. You must show how you arrived at your answers to receive full credit. Any cheating may result in an "F" in the course and will be referred to Student Affairs for other penalties. No make up exams -- sorry.

Attendance policy: If you miss more than 4 lecture/discussion sessions, you lose (i)1% of course grade for each of the next two (5th and 6th) missed lecture/discussion sessions, (ii) 2% of course grade for each of the next two (7th and 8th) missed lecture/discussion sessions, and (iii) 4% of course grade for each of the subsequent (9th onwards) missed lecture/discussion sessions.

Expectations: Attend lectures and discussions, do your homeworks and labs, and BE CURIOUS!

This class may seem mundane for the first few weeks but it will pick up pace quickly. Please do not fall behind early!

Statement on Academic Conduct and Support Systems

Academic Conduct

Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in *SCampus* in Section 11, *Behavior Violating University Standards* https://scampus.usc.edu/1100-behavior-violating-university-standards-and-appropriate-sanctions. Other forms of academic dishonesty are equally unacceptable. See additional information in *SCampus* and university policies on scientific misconduct, http://policy.usc.edu/scientific-misconduct.

Discrimination, sexual assault, and harassment are not tolerated by the university. You are encouraged to report any incidents to the *Office of Equity and Diversity* http://equity.usc.edu or to the *Department of Public Safety* http://capsnet.usc.edu/department/department-public-safety/online-forms/contact-us. This is important for the safety of the whole USC community. Another member of the university community – such as a friend, classmate, advisor, or faculty member – can help initiate the report, or can initiate the report on behalf of another person. *The Center for Women and Men* http://www.usc.edu/student-affairs/cwm/ provides 24/7 confidential support, and the sexual assault resource center webpage http://sarc.usc.edu describes reporting options and other resources.

Support Systems

A number of USC's schools provide support for students who need help with scholarly writing. Check with your advisor or program staff to find out more. Students whose primary language is not English should check with the *American Language Institute* http://dornsife.usc.edu/ali, which sponsors courses and workshops specifically for international graduate students. *The Office of Disability Services and Programs* http://sait.usc.edu/academicsupport/centerprograms/dsp/home_index.html provides certification for students with disabilities and helps arrange the relevant accommodations. If an officially declared emergency makes travel to campus infeasible, *USC Emergency Information* *http://emergency.usc.edu* will provide safety and other updates, including ways in which instruction will be continued by means of blackboard, teleconferencing, and other technology.

New Syllabus

Wk	Tuesday	Thursday	Readings	Lab/Disc
1	Analog vs. Digital Positional # Systems	Number Conversion Binary, Octal, Hex Binary Codes: ASCII, BCD Binary Arithmetic	**W**: Ch. 1, 2.1-2.4, 2.10, 2.12 **LN**: 1-28	Modelsim tool setup, Review
2	Signed Magnitude 2's complement System Sign Extension **Postponed**	**The Basics**: Logic Functions & Representation Minterms / Maxterms Canonical Sums/Products	**W**: 2.5,4.1 **LN**: 29-51	Review
3	**The Tools**: Boolean Algebra (T1-T5) Boolean Algebra (T6-T11) DeMorgan's Theorem	**Circuit Analysis** Waveforms (postponed) Conversion to Canonical Form	**W**: 4.1,4.2 **LN**: 51-82	Review
4	Design Goals Circuit Design, Manipulations, 2-Level Implementations **Circuit Synthesis** Canonical Implementation	Simplified 2-Level Impl. Karnaugh Maps Don't Cares	**W**: 4.3, 9.1 **LN**: 83-1	K-Maps
5	Decoders and Muxes	Decoders (Enables, Active Levels, Composition), Multiplexers (Composition, Width)	**W**: 6.4, 6.7 **LN**: 129-140, 144-156	
6				
7				Quiz
Quiz - 2/26/2016 2-3:50PM				
8				
9				
10				
11				
Midterm – 4/1/2016 2-3:50PM				
13			-	
14			-	
15		Final Review	-	
Final Exam (Cumulative): Tues., May 10th from 10:30AM-1:30PM. Location TBA				

OLD Syllabus

OLD Syllabus (we are trying to change this)
EE 101 Schedule and Topics (W = Wakerly, LN = Lecture Notes)

Wk	Tuesday	Thursday	Readings	Lab/Disc
1	Analog vs. Digital Positional # Systems	Number Conversion Binary, Octal, Hex Binary Codes: ASCII, BCD Binary Arithmetic	**W**: Ch. 1, 2.1-2.4, 2.10, 2.12 **LN**: 1-28	Modelsim tool setup, Review
2	Signed Magnitude 2's complement System Sign Extension	**The Basics**: Logic Functions & Representation Minterms / Maxterms Canonical Sums/Products	**W**: 2.5,4.1 **LN**: 29-51	Review
3	**The Tools**: Boolean Algebra (T1-T5) Boolean Algebra (T6-T11) DeMorgan's Theorem	**Circuit Analysis** Waveforms (maybe timing) Conversion to Canonical Form	**W**: 4.1,4.2 **LN**: 51-82	Review
4	Design Goals Circuit Design, Manipulations, 2-Level Implementations **Circuit Synthesis** Canonical Implementation	Simplified 2-Level Impl. Karnaugh Maps Don't Cares Decoders & Muxes & ROM's	**W**: 4.3, 9.1 **LN**: 83-125	K-Maps
5	More Circuit Design	Decoders (Enables, Active Levels, Composition)	**W**: 6.1, 6.4 **LN**: 126-140	
6	Encoders Multiplexers (Composition, Width)	Multiplexers Demultiplexers Adders	**W**: 6.5, 6.7, 6.10 **LN**: 140-156	Quiz
Quiz - 2/26/2016 2-3:50PM				
7	Adders Multipliers	Addition/Subtraction Overflow	**W**: 6.10-6.11, 2.5-2.6 **LN**: 157-182	
8	Comparators XOR's & Parity	Sequential Logic Bistables	**W**: 6.9, 6.8,6.6,7.1 **LN**: 183-195	
9	Latches Flip-Flops	Master/Slave FF's Review	**W**: 7.1, 7.2 **LN**: 195-222	
10	State Machine Overview State Machine Analysis	State Machine Design State Machine Analysis	**W**: 7.2-7.3 **LN**: 223-233	Review
11	State Machine Design Registers Registers W/ Enables	Counters Digital System Design	**W**: 7.3-7.5 **LN**: 234-255	
Midterm – 4/1/2016 2-3:50PM				
12	Datapath & ALU design	System Design (Vending Machine)	**W**: 8.2, 8.4, 8.5 **LN**: 255-280	
13			-	
14			-	
15		Final Review	-	
Final Exam (Cumulative): Tues., May 10th from 10:30AM-1:30PM. Location TBA				

* Schedule tentative. Expected to change substantailly. *