Fall 2014 **EE 457 Syllabus** **Instructor: Gandhi Puvvada**

Computer Systems Organization

0. Preparation before the first day of classes: Welcome to the EE457 course in Fall 2014. I am providing the following first 3-weeks' material in advance so that some of you can benefit from it.

Study Plan for the first 3 weeks
http://www-classes.usc.edu/engr/ee-s/457/EE457_Study_Plan_for_first_3_weeks.docx
http://www-classes.usc.edu/engr/ee-s/457/EE457_Study_Plan_for_first_3_weeks.pdf

1. Abstract: This course covers computer organization and design. It provides CS/CE/EE students a substantial understanding of a CPU at its logic design level. Design of the control unit and the data path unit of a simple multi-clock-cycle CPU and a pipelined CPU is covered in detail. Hardware support for exceptions, dynamic scheduling of instructions (Tomasulo algorithm to execute instructions in an out-of-order fashion), and branch prediction are also discussed. Computer arithmetic and memory hierarchies (cache, main memory, virtual memory) are also covered. Hardware-software interface is discussed. Students design in Verilog and use ModelSim simulator to verify their design/simulation exercises.

At the end of the course, students are expected to feel confident to perform logic design of a CPU or any hardware system utilizing pipelining and other RTL techniques and proceed to graduate courses in computer architecture or general hardware design.

2. Course administration

a) Course prerequisites: EE254L (EE201L) Introduction to Digital Circuits and EE357 Basic Organization of Computer Systems are the *necessary* prerequisites. Undergraduate students without these prerequisites will not be able to do this course. Graduate students are expected to have taken a logic design course and a course covering some assembly language in their undergraduate course work before taking this course.

b) Classes: http://classes.usc.edu/term-20143/classes/ee-457

Discussion class is *not optional*. The homeworks and the lab assignments are primarily discussed during the discussion class. Important additional material may be covered in the discussion class.

c) Examinations: No makeup exams.

Please note that EE457 exams are long as they are design exams. I do not want to hurry you up. So please cooperate with me and allow me to extend the exam time to 2H 50 minutes.

One quiz (~10%), one midterm (~20%), and the final exam (~30%)

The "Quiz" slot (Qz 10:00 – 11:50 AM Friday, extended to **09:00**-11:50AM)
We will utilize this slot only twice in the whole semester to conduct a quiz and a midterm exam. So it is OK to have schedule conflict with the quiz slot provided you agree to make yourself available for these two occasions.

Quiz (~10%): Friday Sept. 26, 2014 09:00 AM - 11:50 AM PST (the extended quiz slot).
Exam Halls: _____.

Midterm (~20%): Friday Oct. 31, 2014 09:00 AM - 11:50 AM PST (the extended quiz slot).
Exam Halls: _____.

Nov 14	Last day to drop a class with a mark of "W"

http://classes.usc.edu/term-20143/calendar/

Final Exam (~30%): Wednesday, Dec 17, 2014 07:30-10:20 AM PST Exam Hall _____

Extended time slot (Starting time is adjusted to **7:30AM** and end time is adjusted to **10:20AM**
Hope none of you have any conflict with this (30+20=) 50 min. extension.
Note: EE457 Final Exam is as per the Exceptions Schedule posted at the bottom of:
http://classes.usc.edu/term-20143/calendar/

d) Grading Policy:

Weights of course components:
Quiz: **~10%**, Midterm Exam **~20%** No make-up exams.
Homeworks **10% to 15%** (penalty for late submission: up to 5% per day up to 1 day if solution has not been distributed).
*Design labs** **25% to 30%** (penalty for late submission: 3% flat up to 3 days).
Final exam **~30%** No make-up exam.

* *We will be using* Modelsim Verilog design entry and simulation tools *to do a number of design exercises.*

e) Academic Accommodations:

Any student, requiring academic accommodations based on a disability, is required to register with the Center for Academic Support and Disability Services and Programs (CAS & DSP) each semester.
A letter of verification for approved accommodations can be obtained from CAS & DSP. Please make sure that the letter is delivered to me as early in the semester as possible (no less than 2 weeks before an exam).
The CAS & DSP office is located in STU 301.

Their phone number is (213) 740-0776.
http://sait.usc.edu/academicsupport/centerprograms/dsp/home_index.html

f) Miscellaneous administrative matters:

Lecture class attendance, penalty for absence, and minimum required performance:

If you miss more than 2 lecture meetings, you will start noticing that you are falling behind.
If you miss more than 5 lecture meetings, you may as well drop the course.
It is a design course requiring continuity in your learning process. So, please attend every lecture meeting.
The following penalty rule does not apply to remote students, as I cannot monitor their attendance. They are allowed to watch the lecture in the evening/late night.
Penalty for lecture absence: 1% for 3rd, 4th; 2% for 5th and after.
Penalty for discussion absence: 0.5% for 3rd, 4th; 1% for 5th and after.
http://www-classes.usc.edu/engr/ee-s/457/EE457_attendance_policy.html

Homeworks shall be done individually. Design and simulation labs can be performed either individually or in teams of two students (2 per team). But occasionally, design labs may be assigned as individual assignments.
Teams shall submit one set of Verilog code online.
However justifications/explanations, state diagrams, and answers to questions at the end of the lab assignment and waveforms if asked, shall be prepared individually.
Copying is different from discussing ideas with other students.
You are encouraged to share your thoughts on homework, design labs, and design lab reports with others as long as you act like a Teaching Assistant who tries to help without giving away the solution.
Absolutely no copying. Do NOT try to copy design files. We have ways to find if a design/simulation lab has been copied. Try not submitting a non-working lab as we give very little credit for a non-working lab.
We are here to help you and guide you in your debugging. If you submit a **non-working design/lab** and do not write on the top of it in **BIG** letters that it is NOT WORKING (and further do not inform the instructor, the TAs, and the lab graders through an email before submission), we will treat it as an attempt to cheat. This is very important.

Academic dishonesty cases will be dealt with severely. You must have gone through the short presentation on Academic Integrity at USC posted at
http://www.usc.edu/libraries/about/reference/tutorials/academic_integrity/
http://usclibraries.adobeconnect.com/academicintegrity

Another important resource is the Student Judicial Affairs and Community Standards (SJACS) Website
http://www.usc.edu/student-affairs/SJACS/index.html . You may want to visit
http://www.usc.edu/student-affairs/SJACS/pages/students/community_standards.html
University policy requires that all academic integrity violations are reported to Student Judicial Affairs and Community Standards (SJACS).

We will try to make the assignments due on times far from the class time.
This is to make sure that students do not miss classes to complete their assignments.

Please check your email regularly. Also visit the DEN blackboard (http://www.uscden.net/) regularly.

g) Instructor: Gandhi Puvvada (email: gandhi@usc.edu)
Office: EEB238 Phone: (213) 740-4461
Office hours: http://www-classes.usc.edu/engr/ee-s/457/Gandhi_Office_Hours_Fall2014.pdf
Home phone number: (310) 839-3933 (up to 10:00PM any day including weekends and holidays)

Students are encouraged to discuss any difficulties they are facing in this course with any of us (TAs, Mentors, graders or I).

h) Teaching Assistants Mentors and Graders: We will post their names and office hours on the blackboard under the announcements section.

Please make appointments with the TA(s)/Mentor(s) through email for additional help.

The TAs conduct the discussion sessions. The TAs and the Mentors are primarily responsible for class material, design/simulation labs, end-of-the-lab questions, and homeworks.
For any difficulty with ModelSim or with your simulation exercises, you should first try to approach a TA or a Mentor. If no one is available, you should then contact the instructor. In any case do not delay getting help.

Homework grader can help on homeworks and the lab grader can help on the design/simulation labs and end-of-the-lab questions.
For help on lecture material, it is best to see the instructor.

3. Design/simulation labs schedule:

Approximately one lab (or one part of one lab) will be assigned every week starting from the second week.

The labs make up **25%** to **30%** of your course credit. The weight indicated is tentative.
We may decide to assign quite different points/weights to individual labs.

0) Introduction to Verilog HDL entry and simulation in Modelsim

1) Max. Min. finder State Machine Design Lab #1 Part #1, Part #2, Part #3 (M1, M2, M3, M4)

2) Bubble Sort RTL Exercise Lab #2 Part #1 and Part #2

3) Design of a 32-bit ALU Lab #3
3a) Design of a combinational divider (cancelled)
3b) Design of a special divider (cancelled)

4) Multi-cycle CPU Design Lab #4 Part #4

5) Pipelined Ripple Carry Adder Design Lab #5 (cancelled)

6) Design of a Pipelined CPU Lab #6 Part #5 and Part #4

7) Design of a 3-element adder Lab #7 Part #1, #2,
Design of a simple pipeline Lab 7 Part #3 (Sub parts SP1, SP2)
RTL Coding of a simple pipeline Lab 7 Part #3 (Sub parts SP3, SP3)

4. Readings: The required readings are class notes and sections of the textbook. Please make it a practice to read regularly. It is important to clarify any items that are not clear in that week itself. Students, who postpone reading, gradually drift away from the rest of the class and eventually perform very poorly on the exams and design/simulation labs.

Primary References:

Class Notes (required): Please buy from the university (USC) bookstore.
Remote students can place their orders online for the class notes and other items at the following (They may have to wait for a week to place their order):
USC Bookstores => Book Division => Distance Education
http://uscbookstore.com/courselistbuilder.aspx
If there is any problem, please call (213) 740-TEXT and also let me know if the problem cannot be resolved.

Lab Manual: We prefer to distribute the lab assignments progressively as pdf files. We can review and revise each assignment (if needed) and post it on the Blackboard.

Textbook/Verilog Guide:
1. Computer Organization & Design - The Hardware and Software Interface 5th edition
By D. A. Patterson (Berkeley) and J. L. Hennessey (Stanford)
You can buy it from the university (USC) bookstore or any place (such as online bookstores).
http://store.elsevier.com/Computer-Organization-and-Design/David-Patterson/isbn-9780124077263/
If you have the 4th edition, that is fine too.

2. The Verilog 2001 Reference Guide by Esperan (Cadence)
You need this for your Verilog-based design/simulation labs. **You can use it in the EE457 exams**. Esperan (Cadence) does not sell it to individuals. They provided to USC the pdf file free. I will bring a few printed copies to the exam hall and you can borrow a copy for a short time.

Secondary References (Do not buy these):

1. EE101 and EE254L (EE201L) Textbook: Digital Design Principles and Practices By John F. Wakerly
2. EE357 Textbook: Computer Organization by Hamacher
3. Advanced Computer Architecture with Parallel Programming By Kai Hwang
4. Computer Architecture - A Quantitative Approach By D. A. Patterson and J. L. Hennessy
5. Computer Arithmetic Algorithms By Israel Koren

5. Tentative Course Schedule (for a 14-week (28-lecture) Fall/Spring semester):

Chapter numbers point to chapters in my class notes.

# of lectures	Lecture	Item	Homework /Lab
2	1, 2	**Ch#1** Intro to course, review of prerequisite material, Review data path and control unit design, Moore and Mealy, Glitches in control signals, Data registers with Data enable, State diagram design, All Inclusive and Mutually Exclusive rules,	HW#1
0		Verilog coding: Watch the 6-part EE254L lectures at home and learn by yourselves. Install Modelsim and learn to use the tool by yourself	Tools installation
1	3	Compare and contrast: state diagram vs. flow-chart, Min-Max Lab	Lab #1
1	4	**Ch#2** Performance, MIPs, MFLOPs	HW #2
2	5, 6,	**Ch#3** MIPs ISA, SLT, SLTU lw, sw, Byte addressable processors, memory addresses. also cover word addresses in a byte addressable processor	HW #3 cancelled
2	7, 8,	**Ch#4 P1** Review overflow detection in unsigned and signed arithmetic and ALU design	ALU lab Lab #3
2	9, 10,	**Ch#5 P1** Single Cycle CPU, **Ch#5 P2** multi-cycle CPU Datapath and control design	HW #5A Lab 4 Part #4 (Multi-cycle CPU)
0		**Quiz exam** in the Friday quiz slot (time extended **9:00**-11:50AM)	
1	11	**Ch#5 P2** Multi-cycle CPU 2nd edition design	HW #5B
4	12,13, 14, 15	**Ch#6** 5-stage pipeline: data dependency solutions (Compiler solution, HDU & FU), and branch implementations (late branch vs. early branch), branch delay slots. Also cover exceptions.	Pipelining Lab 6 – Part 4
1	16	Make-up	
2	17, 18	**Ch#7 P1** Cache: Mapping techniques, CPU address division into fields and connect address to Cache Data RAMs, Cache Tag RAMs,.	Cache HW #6

			Pipeline Structural coding lab Lab #7 P1, P2
2	19, 20	**Ch#7 P2** Virtual memory: Multi-level page table, PTBR, principle of inclusion. TLBs, and interleaved main memory	Virtual Memory HW #7
0		**Midterm exam** in the Friday quiz slot (time extended **9:00**-11:50AM)	
1	21	Exceptions, Exception PC and Cause register	
2	22, 23	Out of order execution and Tomasulo Part 1 (IoI_OoE_OoC), WAR and WAW hazards in OoO execution, IFQ (Instruction prefetch queue), dispatch unit, issue queues, issue unit, CDB	
1	24	Brach Prediction, 1-bit and 2-bit predictors, BPB, BTB	
1	25,	Tomasulo Part 2 (IoI_OoE_IoC), ROB, ROB search, Speculative execution and selective flushing if branch was mispredicted, exception handling,	Lab #7 P3 Sub Parts 1, 2
1	26	**Ch#9** Parallel processing, semaphores, Read-Modify-Write (RMW) race, atomic operations on shared variables, CMP, CMT, Thread-level parallelism, non-blocking cache, MPI	Pipeline RTL coding lab Lab #7 P3 Sub Parts 3, 4
1	27	Snoopy Cache Coherency protocols, Write through vs. write-back, MSI, MOESI	
1	28	Choices for the last lecture: Sometimes we get to do part of one of the following three topics, sometimes none.	
		Ch#10 Non-linear pipelines	
		Ch#4 P2 RCA, CLA	
		Ch#4 P3 CSA-tree (Wallace tree) multiplier	
		Final exam Dec 17, 2014 7:30 AM – 10:20 AM in the exceptional exam time slot extended in time. Find it at the bottom of **http://classes.usc.edu/term-20143/finals/** Electrical Engineering 457 Wednesday, December 17 8-10 a.m.	

********** Final Examination: Comprehensive with focus on later topics. **********