UNIVERSITY OF SOUTHERN CALIFORNIA
USC VITERBI SCHOOL OF ENGINEERING
MING HSIEH DEPARTMENT OF ELECTRICAL ENGINEERING

EE 536A: #30666R/#30658D **SPRING, 2013**
COURSE SYLLABUS **JOHN CHOMA**

ABSTRACT:

EE 536a is an advanced circuits and systems analysis course that forges a foundation for the more design-intensive analog and mixed signal integrated circuits and systems classes offered in the Graduate Division of the Ming Hsieh Department of Electrical Engineering. It teaches students computationally efficient manual and computer-aided methods for analyzing the electrical dynamics of both linear and nonlinear models of active networks destined for monolithic realization, principally in complementary metal-oxide-semiconductor (CMOS) transistor technologies. More than teaching mere analytical problem solving techniques, the course couches analyses in forms that foster engineering insights that underpin a meaningful characterization and performance assessment of active circuits embedded in high frequency and/or high speed system applications. These insights are fundamental to consistently creative circuit and system design, for they enable realistic comparisons among candidate active devices and among plausible circuit architectures. They are also indispensable to the omnipresent design problem of mitigating the deleterious effects that parasitic energy storage and other high order device and circuit phenomena have on such performance metrics as bandwidth, signal delay in both time and frequency domains, gain and phase margins, noise, distortion, and transient responses. In short, the formulation of insightful design-oriented analysis strategies commensurate with the realization of modern integrated circuits, and particularly high performance analog integrated circuits and systems, is the focus of EE 536a.

EE 536a is a design-oriented course that forges the foundation for creative circuit and system realizations. A circuit design venture that culminates by responding positively to the demanding performance specifications of modern data processing, information transmission, and communication systems is a challenging and often daunting undertaking. Design is complicated by the curious fact that computational precision is not the primary objective of design-oriented circuit analysis. Rather, the purpose of analysis is to gain insights into the circuit responses defined by the mathematical solutions for the electrical responses of an electronic circuit. An insightful understanding is cultivated by solutions cast in forms that highlight circuit attributes, limitations, best case operating features, and worst case performance shortfalls. In short, design skills, methodologies, and guidelines are not necessarily nurtured by elegant and mathematically satisfying circuit solutions. They are more likely to derive from approximate circuit solutions that, when properly interpreted in light of given applications, paint an understandable engineering image of pertinent circuit dynamics. EE 536a attempts to paint productive images for the innovative design of high frequency and high speed analog integrated electronics.

In the process of forging realistic design strategies, several fundamental facts and issues are illuminated. The first of these is that integrated circuit design expertise demands more than mere manual and computer-aided circuit analysis skills. In addition to such skills, it requires an understanding of how active device properties and electrical characteristics are implicitly implicated in the problems of accurately predicting and reliably ensuring reproducible circuit and system responses. A second issue uncovered is that the high-speed performance of many electronic networks is not necessarily limited by active device properties. Rather, the high speed performance of circuit structures is often defined by the active and passive energy storage parasitics associated with the metallization interconnects between the output and input ports of two subcircuits, metallization

routing geometries, I/O signal pads, and numerous other circumstances. A third issue is the implicit compromise between high speed device performance and electrical noise generated within these devices. Electrical noise issues are vitally important to integrated circuit design because they effectively define the minimum detectable signal levels that can be reliably processed by a circuit. Although the physical underpinnings of circuit noise phenomena are not explicitly addressed in this course, circuit design strategies aimed toward minimizing the deleterious effects of noise are proffered. Finally, feedback, whether intentional or not, is pervasive of all high speed/broadband systems. Because of the potential instability of closed loop feedback configurations, it follows that the nature and extent of feedback in integrated networks must be thoroughly understood and properly compensated before a design can be finalized.

The foregoing and other design-oriented matters are studied thoroughly in advance of considering specific circuit examples. Included in these example circuits are low noise RF amplifiers, broadband open loop amplifiers, broadband closed loop amplifiers, interstage matching filters, and distributed networks. Preceding the discussion of all of these circuits and systems is a comprehensive study of conventional long channel and short channel models for MOS technologies.

Students enrolled in EE 536a must be comfortable with the technical material traditionally embraced by undergraduate courses on basic circuit theory, system analyses in frequency and time domains, and basic analog electronics in both MOS and bipolar technologies. The computer tools alluded to in the lectures and required in several homework assignments, include SPICE (conventional HSPICE or SPICE versions embedded within CADENCE, TANNER, TOPSPICE, or other design suites), MATLAB, and EXCEL.

1. Course Administration

The prerequisite for *EE 536a* is a baccalaureate degree in electrical engineering and demonstrable competence in introductory circuits courses, linear systems courses, and basic analog electronics. A senior level elective in analog electronics *(EE 479)* is mandated of those who are required to take and do not satisfactorily complete the placement examination administered in advance of class commencement. **Course lectures are given on the USC University Park Campus on Mondays and Wednesdays from 9:30 -to- 10:50 AM in Olin Hall of Engineering (OHE), Room #136**.

EE 536a lectures commence on Monday, 14 January 2013, and end on Wednesday, 01 May 2013. Students who are absent from a given lecture should arrange for a colleague to obtain any notes, homework assignments, homework solutions, or other information that may have been distributed in class or posted on the web during their absence. On the rare occasion when hard copies are disseminated to students, extras of such material are not retained by the instructor. All supplemental course notes, lecture aids (PDF versions of PowerPoint presentations used in formal class lectures) homework assignments, homework solutions, and other information and material can be found at the website, **www.jcatsc.com**.

The last day to drop the course <u>without</u> a *"W"* grade and receive a *100*% refund of assessed course charges is Friday, 01 February 2013. The last day to drop the class <u>with</u> a *"W"* grade is Friday, 12 April 2013. An **Incomplete *"IN"*** course grade is rarely given. An ***"IN"*** grade can be justified only in <u>substantiated exceptional cases</u> such as an extended student illness, a temporary physical disability, or a personal hardship experienced after the twelfth week of the semester (after 12 April 2013).

The final examination is scheduled for Friday, 10 May 2013, from 8:00 AM -to- 10:00 AM. One midterm examination is also planned. A <u>tentative</u> date for the midterm examination, which is announced well in advance of its administration, is Wednesday, 03 March

2013. Optional review sessions in advance of formal examinations and/or as required, which are designed to facilitate comprehension of especially difficult technical material, may be scheduled aperiodically, pending the extent of student interest in such sessions and the availability of an appropriate Distance Education Network (DEN) classroom.

The results of the midterm examination and the final examination combine with averaged homework grades in accordance with the algorithm given below to determine the final course average for each student. It should be noted that a conscientious effort is made to have homework assignments complement lecture material and impending examinations. Homework is assigned periodically, and solutions are normally posted at **www.jcatsc.com** by the day following the day on which assignments are handed in for grading.

MIDTERM EXAMINATION GRADE:	**20%**
DESIGN/ANALYSIS PROJECT:	**25%**
FINAL EXAMINATION GRADE:	**40%**
HOMEWORK GRADE:	**15%**

Examinations can never be made up, nor can they be administered in advance of the scheduled examination date unless suitable arrangements are made with the course instructor. **The date and time of the final examination is established by University Administration and in general, they cannot be altered.** If a student fails to take the midterm examination, his or her grade is based on a normalized maximum possible score of *80*, as opposed to the traditional maximum of *100*. **An automatic failure results if the student has a non-excused absence from the final examination**.

Prof. John Choma is the Course Lecture Instructor; the probable Discussion Leader is Mr. Aaron Curry. Prof. Choma's office hours are difficult to predict accurately and reproducibly but generally, they are nominally from 12:00 -to- 1:30 on Mondays and from 1:00 -to- 2:30 on Tuesdays in Powell Hall of Engineering **(PHE) Room #620**. Appointments for other meeting times can be arranged easily by telephoning Prof. Choma at **213-740-4692** or by e-mailing him at **johnc@usc.edu**. Discussion Leader will also establish regular office hours.

2. Discussion Sections

Weekly discussion sections spearheaded by the Discussion Leader are scheduled for **Wednesdays from 5:00 -to- 5:50 PM in Olin Hall of Engineering (OHE), Room #136**. These discussion sessions will be aired to all remote Distance Education Network (DEN) students. Additional and optional discussion sections may also be established as the semester progresses. Homework assignments are addressed in the discussion sections, as is particularly challenging lecture material. During the first week of the spring 2013 semester, no Discussion Sections will meet.

3. Student Preparation

The student is directed to *CHAPTER ONE* of the assigned textbook. This chapter comprises a review of essentially all undergraduate circuits and systems concepts whose understanding is deemed a pivotally important prerequisite to the satisfying assimilation of EE 536a lecture material. There are no plans to cover this first chapter material as an explicit component of

formal class lectures. Nevertheless, EE 536a students are held responsible for the technical content therein.

4. Study Guidelines and Suggestions

4.1. Spend time reading the *Abstract* of this Course Syllabus, which defines the pedagogy of the course. Conscientious and properly focused students should understand that solutions to engineering analysis and design problems are not the dominant study issue. Particularly important is the ability to develop the insights that enable insightful interpretations of these solutions so that the fruits of analyses foster innovative circuit and system design skills. A matter related to interpretive acuity is the development of capabilities for defining, applying, and assessing meaningful analytical approximations, which are all but mandated if mathematical tractability and engineering understandability are to be assured.

4.2. It is imprudent to view the *15%* weight attached to homework as being sufficiently small to warrant tacit indifference to these assignments. When diligently addressed and considered, the assigned problems provide analytical experience and engineering insights that are likely to prove beneficial for completing the formal examinations. It should also be understood that homework is counted in the compilation of the final course grade only when its average score enhances the final course average. When the homework average degrades an individual final course average, the homework score is not factored into the overall course average, which is then based on an achievable maximum score of *85%*, as opposed to *100%*. In a word, homework scores can only help the student's final grade.

4.3. Engineers rarely work independently. Accordingly, students are encouraged to work in small teams (no larger than four) on homework assignments, assuming, of course, that such collaboration is done intelligently, conscientiously, and in a manner that encourages equal and proactive participation among all group members. Homework teams need only hand in one assignment per group, making sure that the first page of each submitted assignment clearly identifies the names and corresponding student identification numbers of all group participants. Each member of a given group receives the same numerical mark for the given submission. Homework assignments are graded by the Discussion Leader. On the other hand, examinations are graded exclusively by Prof. Choma.

4.4. Do not fall behind in the course lectures and assignments! Advanced electrical engineering classes, such as EE 536a, are hierarchical; that is, the ability to understand material presented in any given week relies strongly on the comprehension of relevant technical matter discussed in preceding lectures or addressed in earlier assignments.

4.5. Try not to miss any scheduled class or any supplementary discussion sections that may be offered! Graduate courses tend to inspire discussions of important tangential material that may not be explicitly addressed in the assigned readings.

4.6. Do not be shy in the classroom about asking questions about material that is not clearly comprehended. If something is not well understood, chances are that many others in class are experiencing similar confusion. Do not be shy about asking for additional assistance and visiting Prof. Choma during regular office hours or at times arranged by appointment.

5. Required Readings and Suggested References

The required textbook is as follows:

J. Choma and W-K. Chen, *Feedback Networks: Theory and Circuit Applications*. Singapore: World Scientific Press, 2007 [ISBN Number 978-981-02-2770-8 or ISBN Number 10--981-02-2770-1]. The assigned chapter readings in the Course Schedule refer to this text. PDF versions of relevant textual course notes are made available to the student at **www.jcatsc.com**. These are delineated in the Course Schedule as "Course Notes." Additionally, PDF versions of actual PowerPoint

class lectures are made similarly available. These are delineated in the Course Schedule as "Lecture Aids."

The following textbooks contain potentially beneficial reference reading material.

RECOMMENDED TEXTBOOKS

Phillip E. Allen and Douglas R. Holberg, *CMOS Analog Circuit Design*. New York: Oxford University Press, 2002.

Norman Balabanian and Theodore Bickart, *Linear Network Theory: Analysis, Properties, Design and Synthesis*. Beaverton, Oregon: Matrix Publishers, Inc., 1981.

M. J. Buckingham, *Noise in Electronic Devices and Systems*. Chichester, United Kingdom: Ellis Harwood Limited Publishers, 1983.

Mark Burns and Gordon Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*. New York: Oxford University Press, 2001.

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J. Choma, Jr., *Electrical Networks*. New York: Wiley–Interscience, 1985.

K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*. Reading, Massachusetts: Addison-Wesley Pub. Co., 1978.

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Robert E. Collin, *Foundations for Microwave Engineering*. New York: McGraw-Hill Book Co., 1966.

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Roger T. Howe and Charles G. Sodini, *Microelectronics: An Integrated Approach*. Upper Saddle River, New Jersey: Prentice Hall, Inc., 1997.

Johan H. Huijsing, Rudy J. van der Plassche, and Willy Sansen (editors), *Analog Circuit Design*. Boston: Kluwer Academic Publishers, 1993.

Mohammed Ismail and Terri Fiez (editors), *Analog VLSI Signal And Information Processing*. New York: McGraw-Hill, Inc., 1994.

Richard C. Jaeger, *Microelectronic Circuit Design*. New York: McGraw-Hill, 1997.

D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: John Wiley and Sons, Inc., 1997.

Kenneth R. Laker and Willy M. C. Sansen, *Design of Analog Integrated Circuits and Systems*. New York: McGraw-Hill, Inc., 1994.

B. P. Lathi, *Modern Digital and Analog Communication Systems*. New York: Oxford University Press, 1998.

William Liu, *MOSFET Models for SPICE Simulation*. New York: John Wiley and Sons, Inc., 2001.

Gaetano Palumbo and Salvatore Pennisi, *Feedback Amplifiers: Theory and Design*. Boston: Kluwer Academic Publishers, 2002.

Sunggu Lee, *Design of Computers and Other Complex Devices*. Upper Saddle River, New Jersey: Prentice-Hall, 2000.

Thomas H. Lee, *The Design Of CMOS Radio–Frequency Integrated Circuits*. Cambridge, United Kingdom: Cambridge University Press, 2004.

William Liu, *MOSFET Models for SPICE Simulation, Including BSIM3v3 and BSIM4*. New York: Wiley-Interscience, 2001.

Edgar Sánchez-Sinencio and Andreas G. Andreou (editors), *Low–Voltage/Low–Power Integrated Circuits and Systems*. New York: IEEE Press, 1999.

Thomas F. Schubert, Jr. and Ernest M. Kim, *Active and Non–Linear Electronics*. New York: John Wiley & Sons, Inc., 1996.

G. C. Temes and J. W. LaPatra, *Introduction to Circuit Synthesis and Design*. New York: McGraw-Hill Book Company, 1977.

Annon Yariv, *Optical Electronics in Modern Communications*. New York: Oxford University Press, Inc., 1997.

The following information is a partial list of relevant classic journal literature organized loosely among the indicated topical areas.

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CIRCUIT DESIGN METHODS AND EXAMPLES

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P. Allen and M. B. Terry, "Use of Current Amplifiers For High Performance Voltage Applications," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 155-162, 1980.

M. Atarodi and J. Choma, Jr., "A 7.2 GHz Bipolar Operational Transconductance Amplifier For Fully Integrated OTA-C Filters," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 6, pp. 243-253, Nov. 1994.

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B. M. Ballweber, R. Gupta, and D. J. Allstot, "A Fully Integrated 0.5-5.5 GHz CMOS Distributed Amplifier," *IEEE J. Solid-State Circuits*, vol. 35, pp. 231-239, Feb. 2000.

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6. Course Schedule

WEEK	WEEK OF	LECTURE TOPIC	READINGS
1, 2, 3	01/13/2013 01/20/2013 01/27/2013	MOS TECHNOLOGY MODELS & APPLICATIONS Subthreshold Regime Ohmic (Triode) Regime Saturation Regime Model Relationship to Device Cross Section Transistor Capacitances Short Channel Devices *Horizontal Electric Field Effects* *Vertical Electric Field Effects* *Threshold Voltage Modulation* *Channel Length Modulation* *Temperature Effects* Example Common Source Amplifier Gilbert Multiplier	Course Notes 1 Lecture Aid 1 Chapter 7
4, 5	02/03/2013 02/10/2013	MOSFET CIRCUIT BIASING Voltage and Current References *Diode and Active Voltage Dividers* *Low Voltage Biasing* *Low Voltage Cascode* Supply-Independent Biasing *Constant Transconductance* *Circuit Startup Requirements* *Feedback Parameter* Bandgap Reference *PN Junction Thermal Characteristics* *Circuit Realizations* Adaptive Biasing *Linearity Restrictions of Differential Pairs* *Adaptive Network Realization*	Course Notes 2 Lecture Aid 2
6	02/17/2013 *[Cursory Review Only Is Given In Class]*	CANONIC ANALOG MOSFET CELLS Common Source Amplifier *Biasing Subcircuits* *Source Degeneration* *CMOS Cell* Common Drain Amplifier *Active Load* *Common Source Buffering* Common Drain Amplifier *Common Source-Common Gate Cascode* *Regulated Cascode* *Folded Cascode* Balanced Differential Amplifier *Half Circuit Models* *I/O Impedance Representations*	Lecture Aid 3 Course Notes 3 Chapter 7 Chapter 8

WEEK	WEEK OF	LECTURE TOPIC	READINGS
6	02/17/2013	*Differential -To- Single-Ended Converter*	
7	02/24/2013	FEEDBACK CIRCUITS (SYSTEM LEVEL) Feedback Network Frequency Response *Single Pole Response* *Second Order Response* Stability Issues *Phase Margin* *Gain Margin* *Compensation*	Chapter 4 Chapter 5 Chapter 6 Lecture Aid 4 Lecture Aid 5
8, 9, 10	03/03/2013 03/10/2013 03/24/2013	Signal Flow Analysis Methods *Null Parameter Gain* *Return Ratio* *Null Return Ratio* *I/O Impedance Levels* Feedback Topologies *Global and Local Feedback* *Dual Loop Feedback* Circuit Examples	Chapter 4 Chapter 5 Chapter 6 Lecture Aid 5 Lecture Aid 10
9	**03/13/2013**	***MIDTERM EXAMINATION***	***Open Notes & Book***
	03/17/2013	****SPRING BREAK ******	***NO CLASS***
11	03/31/2013 *[Abbreviated Discussions]*	CANONIC CELLS AT HIGH FREQUENCIES Common Source Amplifier *I/O Gain Frequency Response* *I/O Impedance Frequency Responses* *Active Loads* Common Drain Amplifier *I/O Gain Frequency Response* *I/O Impedance Frequency Responses* *Active Loads* Common Gate Amplifier *Low Frequency Characteristics* *High Frequency Properties* Transconductor Amplifiers	Chapter 7 Chapter 8 Lecture Aid 6
11, 12	03/31/2013 04/07/2013	BROADBAND AND RF AMPLIFIERS Pole Dominance Degenerative RC Broadbanding Response Peaking *Shunt Peaking* *Series Peaking* *Series-Shunt Peaking* Feedback Broadbanding Narrowband Tuning *Common Source RF* *Active Gate Impedance Compensation* *Frequency Response*	Chapter 9 Lecture Aid 7 Course Notes 4 Course Notes 5
13, 14, 15	04/14/2013 04/21/2013 04/28/2013	ELECTRICAL NOISE Noise Analysis Strategies *Time Domain Representation* *Frequency Domain Representation*	Lecture Aid 11 Tech. Reports

WEEK	WEEK OF	LECTURE TOPIC	READINGS
		Two-Port Network Models	
		Network Cascades	
		Noise In Devices	Tech. Reports
		Johnson(Thermal) Noise	
		Shot Noise	
		Flicker Noise	
		Noise In Subthreshold MOS	Tech. Reports
		Noise In Analog Canonic Cells	Tech. Reports
15	04/28/2013	*Common Drain Amplifier*	
		Source Follower	
		Common Gate Amplifier	
	05/10/2013 Last Class, 05/01/2013	***FINAL EXAMINATION (8:00AM –10:00 AM)***	***Open Notes, Open Book***

Dr. John Choma,
Professor of Electrical Engineering
Ming Hsieh Department of Electrical Engineering
03 November 2012

cc. Prof. E-S. Kuh, Department Chair
Dr. Edward Maby, Associate Department Chair
EE 536a–Website