UNIVERSITY OF SOUTHERN CALIFORNIA
USC VITERBI SCHOOL OF ENGINEERING
MING HSIEH DEPARTMENT OF ELECTRICAL ENGINEERING

EE 536A: #30695D/#30696D **FALL SEMESTER, 2012**
COURSE SYLLABUS **CHOMA**

ABSTRACT:

EE 536a is an advanced circuits and systems analysis course that forges a foundation for the more design-intensive analog and mixed signal integrated circuits and systems classes offered in the Graduate Division of the Ming Hsieh Department of Electrical Engineering. It teaches students computationally efficient manual and computer-aided methods for analyzing the electrical dynamics of both linear and nonlinear models of active networks destined for monolithic realization, principally in complementary metal-oxide-semiconductor (CMOS) transistor technologies. More than teaching mere analytical problem solving techniques, the course couches analyses in forms that foster the engineering insights that underpin a meaningful characterization and performance assessment of active circuits embedded in high frequency and/or high speed system applications. These insights are fundamental to creative circuit and system design, for they enable realistic comparisons among candidate active devices and among plausible circuit architectures. They are also indispensable to the omnipresent design problem of mitigating the deleterious effects that parasitic energy storage and other high order device and circuit phenomena have on such performance metrics as bandwidth, signal delay in both time and frequency domains, gain and phase margins, noise, distortion, and transient responses. In short, the formulation of insightful design-oriented analysis strategies commensurate with the realization of modern, high performance, analog integrated circuits and systems, is the focus of EE 536a.

EE 536a is a design-oriented course that forges the foundation for creative circuit and system realizations. A circuit design venture that culminates by responding positively to the demanding performance specifications of modern data processing, information transmission, and other forms of signal processing and communication systems is a challenging and often daunting undertaking. Design is complicated by the curious fact that computational precision is not the primary objective of design-oriented circuit analysis. Rather, the purpose of analysis is to gain insights into the circuit responses defined by the mathematical solutions for the electrical responses of an electronic circuit. An insightful understanding is cultivated by solutions cast in forms that highlight circuit attributes, limitations, best case operating features, and worst case performance shortfalls. In short, design skills, methodologies, and guidelines are not necessarily nurtured by elegant and mathematically satisfying circuit solutions. They are more likely to derive from approximate circuit solutions that, when properly interpreted in light of given applications, paint an understandable engineering image of pertinent circuit dynamics. EE 536a attempts to paint productive images for the innovative design of high frequency analog integrated electronics.

In the process of forging realistic design strategies, several fundamental facts and issues are illuminated. The first of these is that integrated circuit design expertise demands more than mere manual and computer-aided circuit analysis skills. In addition to such skills, it requires an understanding of how active device properties and electrical characteristics are implicitly implicated in the problems of accurately predicting and reliably ensuring reproducible circuit and system responses. A second issue uncovered is that the high-speed performance of many electronic networks is not necessarily limited by active device properties. Rather, high speed circuit performance is often bracketed by the active and passive energy storage parasitics associated with the metallization interconnects between the output and input ports of two subcircuits. A third issue is the invariable

compromise between high speed device performance and electrical noise generated within these devices. Electrical noise issues are vitally important to integrated circuit design because they define the minimum detectable signal levels that can be reliably processed by a circuit. Although the physical underpinnings of circuit noise phenomena are not explicitly addressed in this course, circuit design strategies aimed toward minimizing the deleterious effects of noise are proffered. Finally, feedback, whether intentional or not, is inherent in high speed systems. Because of the potential instability of closed loop feedback configurations, it follows that the nature and extent of feedback in integrated networks must be thoroughly understood and properly compensated, as required, before design finalization.

The foregoing and other design-oriented issues are studied thoroughly in advance of considering specific circuit examples. Included in these example circuits are low noise RF amplifiers, broadband open loop and closed loop amplifiers, interstage matching filters, and distributed networks. Preceding the discussion of all of these circuits and systems is a comprehensive study of conventional long channel and short channel models for MOS technologies.

Students enrolled in EE 536a must be comfortable with the technical material traditionally embraced by undergraduate courses on basic circuit theory, system analyses in frequency and time domains, and basic analog electronics in both MOS and bipolar technologies. The computer tools alluded to in the lectures and required in several homework assignments, include SPICE (conventional HSPICE or SPICE versions embedded within CADENCE, TANNER, TOPSPICE, or other design suites), MATLAB, and EXCEL.

1. Course Administration

The prerequisite for *EE 536a* is a baccalaureate degree in electrical engineering and demonstrable competence in introductory circuits courses, linear systems courses, and basic analog electronics. A senior level elective in analog electronics *(EE 479)* is mandated of those who are required to take and do not satisfactorily complete the placement examination administered in advance of class commencement. **Course lectures are given on the USC University Park Campus on Mondays and Wednesdays from 9:30 -to- 10:50 AM in Olin Hall of Engineering (OHE), Room #100B**.

EE 536a lectures commence on Monday, 27 August 2012, and end on Wednesday, 05 December 2012. Students who are absent from a given lecture should arrange for a colleague to obtain any notes, homework assignments, homework solutions, or other information that may have been distributed in class or posted on the web during their absence. On the rare occasion when hard copies are disseminated to students, extras of such material are not retained by the instructor. All supplemental course notes, lecture aids, which are PDF versions of PowerPoint presentations used in formal class lectures, homework assignments, homework solutions, and other information and material can be found at the website, **www.jcatsc.com**.

The last day to drop the course without a *"W"* grade and receive a *100%* refund of assessed course charges is Friday, 14 September 2012. The last day to drop the class with a *"W"* grade is Friday, 16 November 2012. An **Incomplete *"IN"*** course grade is rarely given. An ***"IN"*** grade can be justified only in substantiated exceptional cases such as an extended student illness, a temporary physical disability, or a personal hardship experienced after the twelfth week of the semester (after 16 November 2012).

The final examination is scheduled for Monday, 17 December 2012, from 11:00 AM -to- 1:00 PM. Please read carefully and understand the *Instructions* and *Make-up Final Examinations Policy* posted at

http://www.usc.edu/academics/classes/term_20123/finals.html.

One midterm examination is also planned. A tentative date for the midterm examination, which is announced well in advance of its administration, is **Wednesday, 24 October 2012**. Optional review sessions in advance of formal examinations and/or optional sessions encouraged by lecture material that is viewed as challenging by officially enrolled students, may be scheduled aperiodically, pending the extent of student interest in such sessions and the availability of an appropriate Distance Education Network (DEN) classroom.

The results of the midterm examination and the final examination combine with averaged homework grades in accordance with the weighting given below to determine the final course average for each student. It should be noted that a conscientious effort is made to have homework assignments complement lecture material and impending examinations. Homework is assigned periodically, and solutions are normally posted at **www.jcatsc.com** by the day immediately following the day on which assignments are handed in for grading.

MIDTERM EXAMINATION GRADE:	**20%**
DESIGN PROJECT:	**25%**
FINAL EXAMINATION GRADE:	**40%**
HOMEWORK GRADE:	**15%**

Examinations can never be made up, and homework solutions cannot be accepted late. If a student fails to take the midterm examination, his or her grade is based on a normalized maximum possible score of *80*, as opposed to the traditional maximum of *100*. **An automatic failure results if the student has a non-approved or non-excused absence from the final examination**.

Prof. John Choma is the Course Lecture Instructor. The Discussion Leader is Mr. Uldric Antao. Prof. Choma's office hours are difficult to predict consistently and accurately but generally, they are nominally from 1:00 -to- 2:30 on Mondays and from 10:30 -to- 12:00 on Tuesdays in Powell Hall of Engineering **(PHE) Room #620**. Appointments for other meeting times can be arranged by e-mailing Prof. Choma at johnc@usc.edu. Uldric Antao will also establish regular office hours and provide his contact information.

2. Discussion Sections

Weekly discussion sections spearheaded by the Discussion Leader are scheduled for Fridays from 10:00 -to- 10:50 AM in Olin Hall of Engineering (OHE), Room #120. These discussion sessions are transmitted to all remote Distance Education Network (DEN) students. Additional and optional discussion sections may also be established, as deemed necessary, as the semester progresses. Homework assignments are addressed in the discussion sections, as is particularly significant and challenging lecture material. **During the first week of the fall 2012 semester, no Discussion Sections will meet**.

3. Student Preparation

The student is directed to *CHAPTER ONE* of the assigned textbook. This chapter comprises a review of essentially all undergraduate circuits and systems concepts whose understanding is deemed pivotally important to the satisfying assimilation of EE 536a lecture material. There are no plans to cover this first chapter material in formal class lectures. Nevertheless,

EE 536a students are held responsible for the technical content therein.

4. Study Guidelines and Suggestions

4.1. Spend time reading the *Abstract* of this **Course Syllabus**. This *Abstract* defines course pedagogy. Conscientious and properly focused students should understand that solutions to engineering analysis and design problems are not the dominant issue in this class. Particularly important is the ability to develop the insights that enable meaningful engineering interpretations of these solutions so that the fruits of analyses foster innovative circuit and system design skills. A matter related to interpretive acuity is the development of capabilities for defining, applying, and assessing meaningful analytical approximations, which are all but mandated by mathematical tractability and engineering understandability.

4.2. It is imprudent to view the *15%* weight attached to homework as being sufficiently small to warrant tacit indifference to these assignments. When diligently addressed and considered, the assigned problems provide analytical experience and engineering insights that are likely to prove beneficial for completing the formal examinations. It should also be understood that homework is counted in the compilation of the final course grade only when its average score enhances the final course average. When the homework average degrades an individual final course average, the homework score is not factored into the overall course average, which is then based on an achievable maximum score of *85%,* as opposed to *100%*. In a word, homework scores can only help the student's final grade.

4.3. Engineers in industry rarely work independently. Accordingly, students are encouraged to work in small teams (no larger than four) on homework assignments, assuming, of course, that such collaboration is done intelligently, conscientiously, and in a manner that encourages equal and proactive participation among all group members. Homework teams need only hand in one assignment per group, making sure that the first page of each submitted assignment clearly identifies the names and corresponding student identification numbers of all group participants. Each member of a given group receives the same numerical mark for the given submission. Homework assignments are graded by the Discussion Leader. On the other hand, examinations are graded exclusively by Prof. Choma.

4.4. Do not fall behind in the course lectures and assignments! Advanced electrical engineering classes, such as EE 536a, are hierarchical; that is, the ability to understand material presented in any given week relies strongly on the comprehension of relevant technical matter discussed in preceding weekly lectures or addressed in earlier assignments.

4.5. Try not to miss any scheduled class or any supplementary discussion sections that may be offered! Graduate courses tend to inspire discussions of important tangential material that may not be explicitly addressed in the assigned readings.

4.6. Do not be shy in the classroom about asking questions about material that is not clearly comprehended. If something is not well understood, chances are that others in class are experiencing similar confusion. Do not be shy about asking for additional assistance and visiting Prof. Choma during scheduled office hours or at times arranged by appointment. Those students who consistently attend the formal course lectures will be given priority with respect to gaining direct access to Prof. Choma during office hours.

5. Required Readings and Suggested References

The required textbook is as follows:

J. Choma and W-K. Chen, *Feedback Networks: Theory and Circuit Applications*. Singapore: World Scientific Press, 2007 [ISBN Number 978-981-02-2770-8 or ISBN Number 10--981-02-2770-1]. The assigned chapter readings in the Course Schedule refer to this text. PDF versions of relevant textual course notes are available to the student at **www.jcatsc.com**. These are delineated in the Course Schedule as "Course Notes." Additionally, PDF versions of actual PowerPoint class lec-

tures are similarly available. These are delineated in the Course Schedule as "Lecture Aids."

The following textbooks contain potentially beneficial reference reading material.

RECOMMENDED TEXTBOOKS

Phillip E. Allen and Douglas R. Holberg, *CMOS Analog Circuit Design*. New York: Oxford University Press, 2002.

Norman Balabanian and Theodore Bickart, *Linear Network Theory: Analysis, Properties, Design and Synthesis*. Beaverton, Oregon: Matrix Publishers, Inc., 1981.

M. J. Buckingham, *Noise in Electronic Devices and Systems*. Chichester, United Kingdom: Ellis Harwood Limited Publishers, 1983.

Mark Burns and Gordon Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*. New York: Oxford University Press, 2001.

W-K.Chen, *Passive and Active Filters*. New York: John Wiley and Sons, 1986.

W-K. Chen, L. O. Chua, J. Choma, Jr., and L. P. Huelsman (editors), *The Circuits And Filters Handbook*. Boca Raton, Florida: CRC/IEEE Press, 1995.

J. Choma, Jr., *Electrical Networks*. New York: Wiley–Interscience, 1985.

K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*. Reading, Massachusetts: Addison-Wesley Pub. Co., 1978.

Dan Clein, *CMOS IC Layout: Concepts, Methodologies, and Tools*. Boston: Butterworth-Heinemann (Newnes), 2000.

Donald T. Comer, *Introduction To Mixed Signal VLSI*. Highspire, Pennsylvania: Array Publishing Co., 1994.

J. A. Connelly and P. Choi, Macromodeling With SPICE. Englewood Cliffs, New Jersey: Prentice-Hall, Inc., 1992.

R. C. Dorf (editor), *The Electrical Engineering Handbook*. Boca Raton, Florida: CRC Press, 1993.

Daniel P. Foty, *MOSFET Modeling With SPICE: Principles and Practice*. Upper Saddle River, New Jersey: Prentice Hall PTR, 1997.

R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI Design Techniques For Analog And Digital Circuits*. New York: McGraw-Hill Publishing Company, 1990.

P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: John Wiley & Sons, Inc., 2001.

A. B. Grebene, *Bipolar and MOS Analog and Integrated Circuit Design*. New York: Wiley–Interscience, 1984.

Roubik Gregorian and Gabor C. Temes, *Analog MOS Integrated Circuits for Signal Processing*. New York: Wiley–Interscience, 1986.

Roger T. Howe and Charles G. Sodini, *Microelectronics: An Integrated Approach*. Upper Saddle River, New Jersey: Prentice Hall, Inc., 1997.

Johan H. Huijsing, Rudy J. van der Plassche, and Willy Sansen (editors), *Analog Circuit Design*. Boston: Kluwer Academic Publishers, 1993.

Mohammed Ismail and Terri Fiez (editors), *Analog VLSI Signal And Information Processing*. New York: McGraw-Hill, Inc., 1994.

Richard C. Jaeger, *Microelectronic Circuit Design*. New York: McGraw-Hill, 1997.

D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: John Wiley and Sons, Inc., 1997.

Kenneth R. Laker and Willy M. C. Sansen, *Design of Analog Integrated Circuits and Systems*. New York: McGraw-Hill, Inc., 1994.

B. P. Lathi, *Modern Digital and Analog Communication Systems*. New York: Oxford University Press, 1998.

William Liu, *MOSFET Models for SPICE Simulation*. New York: John Wiley and Sons, Inc., 2001.

Gaetano Palumbo and Salvatore Pennisi, *Feedback Amplifiers: Theory and Design*. Boston: Kluwer Academic Publishers, 2002.

Sunggu Lee, *Design of Computers and Other Complex Devices*. Upper Saddle River, New Jersey: Prentice-Hall, 2000.

Thomas H. Lee, *The Design Of CMOS Radio–Frequency Integrated Circuits*. Cambridge, United Kingdom: Cambridge University Press, 2004.

William Liu, *MOSFET Models for SPICE Simulation, Including BSIM3v3 and BSIM4*. New York: Wiley-Interscience, 2001.

K. Martin, *Digital Integrated Circuit Design*. New York: Oxford University Press, 2000.

B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.

Edgar Sánchez-Sinencio and Andreas G. Andreou (editors), *Low–Voltage/Low–Power Integrated Circuits and*

Systems. New York: IEEE Press, 1999.
Thomas F. Schubert, Jr. and Ernest M. Kim, *Active and Non–Linear Electronics*. New York: John Wiley & Sons, Inc., 1996.
G. C. Temes and J. W. LaPatra, *Introduction to Circuit Synthesis and Design*. New York: McGraw-Hill Book Company, 1977.
Annon Yariv, *Optical Electronics in Modern Communications*. New York: Oxford University Press, Inc., 1997.

The following information is a partial list of relevant journal literature organized loosely among the indicated topical areas.

ACTIVE FILTERS

M. Banu and Y. P. Tsividis, "An Elliptic Continuous-Time CMOS Filter With On-Chip Automatic Tuning," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 932-938, 1984.
A. Baschirotto, G. Cesura, F. Rezzi, and F. Svelto, "Low-Power BiCMOS Continuous-Time Shaping Filter," *IEEE Trans. on Circuits and Systems–II*, vol. 44, pp. 404-406, May 1997.
Y. Chang, J. Choma, Jr., and J. Wills, "An Active CMOS Image Reject Filter," *Journal of Analog Integrated Circuits And Signal Processing*; vol. 28, pp. 41-49, July 2001.
R. L. Geiger and E. Sánchez–Sinencio, "Active Filter Design Using Operational Transconductance Amplifiers: A Tutorial," *IEEE Circuits and Devices Magazine*, pp. 20-32, March 1985.
M. Ismail, S. V. Smith, and R. G. Beale, "A New MOSFET–C Universal Filter Structure for VLSI," *IEEE Trans. On Circuits and Systems*, vol. 23, pp. 183-194, 1988.

CIRCUIT CONCEPTS, THEORIES, MODELS

A. Arbel, "Multistage Transistorized Current Modules," *IEEE Trans. Circuits and Systems*, vol. CT-13, pp. 302-310, Sept. 1966.
S. H. Chisholm and L. W. Nagel, "Efficient Computer Simulation Of Distortion In Electronic Circuits," *IEEE Trans. Circuit Theory*, vol. CT-20, pp. 742-745, Nov. 1973.
J. Choma, Jr., "A Generalized Bandwidth Estimation Theory for Feedback Amplifiers," *IEEE Trans. Circuits and Systems,* vol. CAS-31, pp. 861-865, Oct. 1984.
J. Choma, Jr., "Gain and Bandwidth Characteristics of a Variable-Gain, Actively Neutralized, Differential Pair," *IEEE Trans. Circuits and Systems*, vol. CAS-33, pp. 66-71, January 1986.
J. Choma, Jr., "Signal Flow Analysis of Feedback Networks," *IEEE Trans. Circuits and Systems*, vol. 37, pp. 455-463, Apr. 1990.
J. Choma, Jr. and S. A. Witherspoon, "Computationally Efficient Estimation of Frequency Response and Driving Point Impedance in Wideband Analog Amplifiers," *IEEE Trans. Circuits and Systems*, vol. CAS-37, pp. 720-728, June 1990.
J. Choma, Jr. "Communication Circuits: Societal Philosophies And Evolving Roles," *IEEE Circuits and Systems Society Newsletter*, vol. 9, p. 1, June 1998.
D. G. Duff and H-C. Poon, "An Analysis of Low-Frequency Second-Order Distortion In Bipolar Transistors Applied To An Amplifier, *IEEE J. Solid-State Circuits*, vol. SC-8, pp. 447-453, Dec. 1973.
P. C. Grossman and J. Choma, Jr., "Large Signal Modeling of HBTs Including Self-Heating and Transit Time Effects," *IEEE Trans. on Microwave Theory and Techniques*, vol. 40, pp. 449-464, March 1992.
P. J. Hurst, "Exact Simulation of Feedback Circuit Parameters," *IEEE Trans. Circuits and Systems*, vol. 38, pp. 1382-1389, Nov. 1991.
P. J. Hurst, "A Comparison of Two Approaches to Feedback Circuit Analysis," *IEEE Trans. Education*, vol. 35, pp. 253-261, Aug. 1992.
P. J. Hurst and S. H. Lewis, "Determination of Stability Using Return Ratios In Balanced Fully Differential Feedback Circuits," *IEEE Trans. On Circuits and Systems*, Part II, vol. 42, pp. 805-817, Dec. 1995.
C–H. Lee, J. Cornish, K. McClellan and J. Choma, Jr., "Current-Mode Approach For Wide Gain Bandwidth Product Architecture," *IEEE Trans. On Circuits And Systems*, Part II, vol. 45, pp. 626-631, May 1998.
F. J. Lidgey and C. Toumazou, "Current-Mode Analogue Signal Processing," *Proc. Bipolar Circuits and Tech. Mtg*., pp. 224-232, 1991.
J. Mahattanakul and C. Toumazou, "A Theoretical Study of the Stability of High Frequency Current Feedback Op-Amp Integrators," *IEEE Trans. Circuits and Systems*, Part I, vol. 43, pp. 2-12, Jan. 1996.
R. G. Meyer, M. J. Shensa, and R. Eschenbach, "Cross Modulation And Intermodulation In Amplifiers At High Frequencies," *IEEE J. Solid-State Circuits*, vol. SC-7, pp. 16-23, Feb. 1972.

S. Narayanan, "Transistor Distortion Analysis Using Volterra Series Representation," *Bell Syst. Tech. J*., vol. 46, pp. 991-1024, May/June 1967.

S. Narayanan, "Intermodulation Distortion Of Cascaded Transistors," *IEEE J. Solid-State Circuits*, vol. SC-4, pp. 97-106, June 1969.

A. Negungadi and T. R. Viswanathan, "Design of Linear CMOS Transconductance Elements," *IEEE Trans. on Circuits and Systems*, vol. 31, pp. 891-894, Oct. 1984.

M. Ohara, Y. Akazawa, N. Ishihara, and S. Konaka, "Bipolar Monolithic Amplifiers For A Gigabit Optical Repeater," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 491-497, Aug. 1985.

A. Payne and C. Toumazou, "Analog Amplifiers: Classification and Generalization," *IEEE Trans. Circuits and Systems*, Part I, vol. 43, pp. 43-50, Jan. 1996.

G. Palumbo and J. Choma, Jr., "An Overview Of Single And Dual Loop Analog Feedback; Part I: Basic Theory," *Journal of Analog Integrated Circuits And Signal Processing*, vol. 17, pp. 175-194, Nov. 1998.

G. Palumbo and J. Choma, Jr., "An Overview Of Single And Dual Loop Analog Feedback; Part II: Design Examples," *Journal of Analog Integrated Circuits And Signal Processing*, vol. 17, pp. 195-219, Nov. 1998.

W. M. Sansen and R. G. Meyer, "Distortion In Bipolar Transistor Variable-Gain Amplifiers," *IEEE J. Solid State Circuits*, vol. SC-8, pp. 275-282, August 1973.

Y. P. Tsividis, "Design Considerations In Single-Channel MOS Analog Integrated Circuits," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 383-391, June 1978.

Y. P. Tsividis, "Integrated Continuous-Time Filter Design—An Overview," *IEEE J. of Solid–State Circuits*, vol. 29, pp. 166-176, Mar. 1994.

M. Vadipour, "Capacitive Feedback Technique for Wide-Band Amplifiers," *IEEE J. Solid State Circuits*, vol. 28, pp. 90-92, Jan. 1983.

E. A. Vittoz, "MOS Transistors Operating In The Lateral Bipolar Mode And Their Applications In CMOS Technology," *IEEE J. Solid State Circuits*, vol. SC-18, pp. 273-279, June 1983.

J. O. Voorman, "Analog Integrated Filters Or Continuous-Time Filters For LSI and VLSI," *Rev. Phys. Appl*., no. 22, pp. 3-14, January 1987.

T. Wakimoto and Y. Akazawa, "A Low-Power Wide-Band Amplifier Using a New Parasitic Capacitance Compensation Technique," *IEEE J. Solid-State Circuits*, vol. 256, pp. 200-206, Feb. 1990.

S. A. Witherspoon and J. Choma, Jr., "The Analysis of Balanced Linear Differential Circuits," *IEEE Trans. on Education*, vol. 38, pp. 40-50, February 1995.

B. A. Wooley, "Automated Design Of DC-Coupled Monolithic Broad-Band Amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-6, pp. 24-34, Feb. 1971.

CIRCUIT DESIGN METHODS AND EXAMPLES

H. E. Abraham and R. G. Meyer, "Transistor Design For Low Distortion At High Frequencies," *IEEE Trans. Electron Devices*, vol. ED-23, pp. 1290-1297, Dec. 1976.

P. Allen and M. B. Terry, "Use of Current Amplifiers For High Performance Voltage Applications," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 155-162, 1980.

M. Atarodi and J. Choma, Jr., "A 7.2 GHz Bipolar Operational Transconductance Amplifier For Fully Integrated OTA-C Filters," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 6, pp. 243-253, Nov. 1994.

C. T. Armijo and R. G. Meyer, "A New Wide-Band Darlington Amplifier," *IEEE J. Solid-State Circuits*, vol. SC-24, pp. 1105-1109, Aug. 1989.

B. M. Ballweber, R. Gupta, and D. J. Allstot, "A Fully Integrated 0.5-5.5 GHz CMOS Distributed Amplifier," *IEEE J. Solid-State Circuits*, vol. 35, pp. 231-239, Feb. 2000.

W. G. Beall and J. Choma, Jr., "Charge-Neutralized Differential Amplifiers," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 1, pp. 33-44, Sept. 1991.

K. H. Chan and R. G. Meyer, "A Low Distortion Monolithic Wide-Band Amplifier," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 685-690, Dec. 1977.

Y. Chang, J. Choma, Jr., and J. Wills, "A CMOS Monolithic Image-Reject Filter," *Journal of Analog Integrated Circuits And Signal Processing*, vol. 28, pp. 43-51, July 2001.

W-K. Chen, "Theory and Design of Distributed Amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-3, pp/ 165-179, June 1968.

J. Choma, Jr., "Temperature Stable Voltage Controlled Current Source," *IEEE Transactions on Circuits and Systems,* Part I, vol. 41, pp. 405-411, May 1994.

J. Choma, Jr. and M. Ismail "Chip Design: Myths, Ideas, and Opportunities," *IEEE Circuits and Devices Magazine*, vol. 13, pp. 9-13, November 1997.

J. B. Couglin, R. J. Gelsing, P. J. Jochems, and H. J. M. van der Laak, "A Monolithic Silicon Wideband Ampli-

fier From DC To 1 GHz," *IEEE J. Solid-State Circuits*, vol. SC-8, pp. 414-419, Dec. 1973.

W. R. Davis and J. E. Solomon, "A High-Performance Monolithic I-F Amplifier Incorporating Electronic Gain Control," *IEEE J. Solid State Circuits*, vol. SC-3, pp. 408-416, December 1968.

M. G. R. Degrauwe, "CMOS Voltage References Using Lateral Bipolar Transistors," *IEEE J. Solid State Circuits*, vol. SC-20, pp. 1151-1157, December 1985.

B. Gilbert, "A New Wideband Amplifier Technique," *IEEE J. Solid State Circuits*, vol. SC-3, pp. 353-365, December 1968.

B. Gilbert, "A Four Quadrant Analog Divider/Multiplier With 0.01% Distortion," *ISSCC Digest Tech. Papers*, vol. SC-3, pp. 284-289, 1983.

E. L. Ginzton, W. R. Hewlett, J. H. Jasberg, and J. D. Noe, "Distributed Amplification," *Proc. IRE*, vol. 36, pp. 956-969, Aug. 1948.

G. Han and E. Sánchez–Sinencio, "CMOS Transconductor Multipliers: A Tutorial," *IEEE Trans. On Circuits And Systems*, Part II: vol. 45, pp. 1550-1563, Dec. 1998.

B. L. Hart and R. W. J. Barker, "A Precision Bilateral Voltage-Current Converter," *IEEE J. Solid State Circuits*, vol. SC-10, pp. 501-503, 1975.

S. R. Jost, "An 850 MHz Current Feedback Operational Amplifier," *Proc. Bipolar Circuits and Tech. Mtg*., pp. 71-74, 1992.

I. A. Koullias, "A Wideband Low-Offset Current-Feedback Op Amp Design," *Proc. Bipolar Circuits and Tech. Mtg*., pp. 120-123, 1989.

K. Kimura, "An MOS Four-Quadrant Analog Multiplier Based on the Multitail Technique Using a Quadritail Cell as a Multiplier," *IEEE Trans. Circuits and Systems*, Part I, vol. 42, pp. 448-454, Aug. 1995.

I. A. Koullias, "A Wideband Low-Offset Current-Feedback Op Amp Design," *Proc. Bipolar Circuits and Tech. Mtg*., pp. 120-123, 1989.

K. A. Kozma, D. A. Johns, and A. S. Sedra, "Automatic Tuning of Continuous-Time Filters Using An Adaptive Filter Technique," *IEEE Trans. Circuits and Systems*, vol. 38, pp. 1241-1248, 1991.

C–H. Lee, K. McClellan, and J. Choma, Jr., "A Supply Noise-Insensitive CMOS PLL With a Voltage Regulator Using a DC–DC Capacitive Converter," *IEEE J. Solid–State Circuits*; Oct. 2001.

C–H. Lee, K. McClellan, and J. Choma, Jr., "A Supply Noise-Insensitive PLL Design Through PWL Behavioral Modeling and Simulation," *IEEE Trans. On Circuits and Systems*, Part II, vol. 48, pp. 1137-1144, Dec. 2001.

L. Luh, J. Choma, Jr., and J. Draper, "A Reduced Delay Method For Improving The Performance Of Sigma–Delta Analog -To- Digital Converters (ADC)," *Journal of Analog Integrated Circuits And Signal Processing*, vol. 30, pp. 207-215, March 2002.

L. Luh, J. Choma, Jr., and J. Draper, "A High Speed Fully Differential Current Switch," *IEEE Trans. On Circuits and Systems*, Part II, vol. 47, pp. 358-363, April 2000.

L. Luh, J. Choma, Jr., and J. Draper, "A Continuous Time Common Mode Feedback Circuit (CMFB) For High Impedance Current–Mode Applications," *IEEE Trans. On Circuits and Systems*, Part II, vol. 47, pp. 363-369, April 2000.

J. A. Mataya, G. W. Haines, and S. B. Marshall, "IF Amplifier Using Cc-Compensated Transistors," *IEEE J. Solid-State Circuits*, vol. SC-3, pp. 401-407, Dec. 1968.

R. G. Meyer and R. A. Blauschild, "A Four-Terminal Wideband Monolithic Amplifier," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 634-638, Dec. 1981.

R. G. Meyer, R. Eschenbach, and R. Chin, "A Wideband Ultralinear Amplifier From DC To 300 MHz," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 167-175, August 1974.

C. S. Park and R. Schaumann, "A High Frequency CMOS Linear Transconductance Element," *IEEE Trans. on Circuits and Systems*, vol. 33, pp. 1132-1138, Nov. 1986.

S. Pipilos, Y. P. Tsividis, J. Fenk, and Y. Papananos, "A Si 1.8 GHz RLC Filter with Tunable Center Frequency and Quality Factor," *IEEE J. Solid–State Circuits*, vol. 31, pp. 1517-1525, Oct. 1996.

V. I. Prodanov and M. H. Green, "A Differential Active Load and Its Applications in CMOS Analog Circuit Designs," *IEEE Trans. on Circuits and Systems*, vol. 44, pp. 265-273, Apr. 1997.

A. Rodríguez-Vázquez and E. Sánchez-Sinencio, "Special Issue On Low-Voltage and Low-Power Analog and Mixed-Signal Circuits and Systems," *IEEE Trans. Circuits and Systems*, Part I, vol. 42, pp. 827-977, Nov. 1995.

A. Rofougaran, G. Cheng, J. J. Rael, J. Y-C. Chang, M. Rofougaran, P. J. Chang, M. Djafari, M-K. Ku, E. W. Roth, And A. A. Abidi, "A Single-Chip 900-MHz Spread-Spectrum Wireless Transceiver in 1-μm CMOS -- Part I: Architecture and Transmitter Design," *IEEE J. Solid-State Circuits*, vol. 33, pp. 515-534, Apr. 1998.

A. Rofougaran, G. Cheng, J. J. Rael, J. Y-C. Chang, M. Rofougaran, P. J. Chang, M. Djafari, J. Min, E. W.

Roth, And A. A. Abidi, "A Single-Chip 900-MHz Spread-Spectrum Wireless Transceiver in 1-μm CMOS -- Part II: Receiver Design," *IEEE J. Solid-State Circuits*, vol. 33, pp. 535-547, Apr. 1998.

D. K. Shaeffer and T. H. Lee, "A 1.4-V, 1.5-GHz CMOS Low Noise Amplifier," *IEEE J. of Solid–State Circuits*, vol. 44, pp. 265-273, Apr. 1997.

J. Silva-Martinez, M. S. J. Steyaert, and W. M. C. Sansen, "A 10.7–MHz 68–dB SNR CMOS Continuous-Time Filter With On-Chip Automatic Tuning," *IEEE J. of Solid–State Circuits*, vol. 27, pp. 1843-1853, Dec. 1992.

W. M. Snelgrove and A. Shoval, "A Balanced 0.9–μm CMOS Transconductance–C Filter Tunable Over the VHF Range," *IEEE J. of Solid–State Circuits*, vol. 27, pp. 314-323, Mar. 1992.

S. Szczepanski, J. Jakusz, and R. Schaumann, "A Linear Fully Balanced CMOS OTA For VHF Filtering Applications," *IEEE Trans. On Circuits And Systems*, Part II: vol. 44, pp. 174-187, March 1997.

Z. Wang and W. Guggenbuhl, "A Voltage-Controllable Linear MOS Transconductor Using Bias Offset Technique," *IEEE J. of Solid–State Circuits*, vol. 25, pp. 315-317, Feb. 1990.

S. L. Wong, "Novel Drain–Based Transconductance Building Blocks for Continuous–Time Filter Applications," *Electron. Lett.*, vol. 25, pp. 100-101, Jan. 1989.

A. Wyszyński, R. Schaumann, S. Szczepanski, and P. Van Halen, "Design of a 2.7 GHz Linear OTA and a 250-MHz Elliptic Filter in Bipolar Transistor-Array Technology," *IEEE Trans. On Circuits And Systems*, Part II: vol. 40, pp. 19-31, Jan. 1993.

ELECTRICAL NOISE

J. Choma, Jr., "A Model For The Computer-Aided Noise Analysis Of Broad-Banded Bipolar Circuits," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 429-435, Dec. 1974.

R. P. Jindal, "Noise Associated With Distributed Resistance of MOSFET Gate Structures in Integrated Circuits," *IEEE Trans. on Electron Devices*, vol. ED-31, pp. 1505-1509, Oct. 1984.

R. G. Meyer and R. A. Blauschild, "A Wide-Band Low-Noise Monolithic Transimpedance Amplifier," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 530-533, Aug. 1986.

S. Moinian and J. Choma, Jr., "The Frequency Response of Bipolar Transistor Noise Figure," *IEEE Trans. Circuits and Systems*, vol. CAS-33, pp. 72-76, January 1986.

Y. Netzer, "The Design Of Low Noise Amplifiers," *Proc. IEEE*, vol. 69, pp. 728-741, June 1981.

C. A. Walton and C. C. Liu, "A Low-Noise Amplifier With Parallel Integrated-Circuit Transistors," *IEEE J. Solid-State Circuits*, vol. SC-6, pp. 415-417, Dec. 1971.

A. Willemsen and N. Bel, "Low Base Resistance Integrated Circuit Transistor," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 245-246, Apr. 1980.

OSCILLATORS

J. Craninckx and M. Steyaert, "Low-Noise Voltage-Controlled Oscillators Using Enhanced LC-Tanks," *IEEE Trans. On Circuits and Systems*, Part II, vol. 42, pp. 794-804, Dec. 1995.

E. Despain and J. Choma, Jr., "A New Monolithic Voltage–Controlled Oscillator," *Journal of Analog Integrated Circuits And Signal Processing*; vol. 26, pp. 103-115, Feb. 2001.

R. Duncan, K. Martin, and A. Sedra, "A 1 GHz Quadrature Sinusoidal Oscillator," *Proc. Custom Integrated Circuits Conf.*, pp. 91-94, 1995.

H. Wu and A. Hajimiri, "Silicon-Based Distributed Voltage-Controlled Oscillators, *IEEE J. Solid-State Circuits*, vol. 36, pp. 1-10, Mar. 2001.

PASSIVE MONOLITHIC COMPONENTS

J. Y.-C. Chang, A. A. Abidi, and M. Gaitan, "Large Suspended Inductors on Silicon and Their Use in a 2–μm CMOS RF Amplifier," *IEEE Electron Device Letters*, vol. 14, pp. 246-248, May 1993.

E. Despain and J. Choma, Jr., "A New Monolithic Variable Capacitor," *Journal of Analog Integrated Circuits And Signal Processing*; vol. 26, pp. 89-102, Feb. 2001.

H. M. Greenhouse, "Design of Planar Rectangular Microelectronic Inductors," *IEEE Trans. Parts, Hybrids, and Packaging*, vol. PHP-10, pp. 101-109, June 1974.

S. S. Mohan, "Modeling, Design, and Optimization of On-Chip Inductors and Transformers," Ph. D. Dissertation, *Stanford University*, 1999.

N. M. Nguyen and R. G. Meyer, "Si IC–Compatible Inductors and LC Passive Filters," *IEEE J. Solid–State Circuits*, vol. 25, pp. 1028-1031, Aug. 1990.

C. P. Yue and S. S. Wong, "On-Chip Spiral Inductors With Patterned Ground Shields for Si-Based RF ICs," *IEEE J. Solid–State Circuits*, vol. 33, pp. 743-752, May 1998.

C. P. Yue and S. S. Wong, "Physical Modeling of Spiral Inductors on Silicon," *IEEE Trans. Electron Devices*, vol. 47, pp. 560-568, Mar. 2000.

A. Zolfaghari, A. Chan, and B. Razavi, "Stacked Inductors and 1 -to- 2 Transformers in CMOS Technology," *Proc. 2000 Custom Integrated Circuits Conference*, session 15.3, May 2000.

6. Course Schedule

WEEK	WEEK OF	LECTURE TOPIC	READINGS
1, 2, 3	08/27/2012 09/03/2012 09/10/2012	MOS TECHNOLOGY MODELS & APPLICATIONS Subthreshold Regime Ohmic (Triode) Regime Saturation Regime Transistor Capacitances Short Channel Devices *Threshold Voltage Modulation* *Channel Length Modulation* *Temperature Effects* *Horizontal Electric Field Effects* *Vertical Electric Field Effects* Example Common Source Amplifier Gilbert Multiplier Including Design Requirements	Course Notes 1 Lecture Aid 1 Chapter 7
4, 5	09/17/2012 09/24/2012	MOSFET CIRCUIT BIASING Voltage and Current References *Diode and Active Voltage Dividers* *Low Voltage Biasing* *Low Voltage Cascode* Supply-Independent Biasing *Constant Transconductance* *Circuit Startup Requirements* *Feedback Parameter* Bandgap Reference *PN Junction Thermal Characteristics* *Circuit Realizations* Common Mode Compensation Via Feedback *Conventional Compensation* *Advanced Compensation Methods* Adaptive Biasing *Linearity Restrictions of Differential Pairs* *Adaptive Network Realization*	Course Notes 2 Lecture Aid 2
6	10/01/2012	CANONIC ANALOG MOSFET CELLS Common Source Amplifier *Biasing Subcircuits* *Source Degeneration* *CMOS Cell* Common Drain Amplifier *Active Load* *Common Source Buffering* Common Drain Amplifier *Common Source-Common Gate Cascode* *Regulated Cascode* *Folded Cascode* Balanced Differential Amplifier *Half Circuit Models* *I/O Impedance Representations*	Lecture Aid 3 Course Notes 3 Chapter 7 Chapter 8 *Largely* *Left To* *The Student* *(Basically* *Undergraduate* *Material)*

WEEK	WEEK OF	LECTURE TOPIC	READINGS
6	10/01/2012	*Differential -To- Single-Ended Converter*	
7	10/08/2012	FEEDBACK CIRCUITS (SYSTEM LEVEL) Feedback Network Frequency Response *Single Pole Response* *Second Order Response* Stability Issues *Phase Margin* *Gain Margin* *Gain Margin* *Compensation*	Chapter 4 Chapter 5 Chapter 6 Lecture Aid 4 Lecture Aid 5 Lecture Aid 4
8, 9, 10	10/15/2012 10/22/2012 10/29/2012	Signal Flow Analysis Methods *Null Parameter Gain* *Return Ratio* *Null Return Ratio* *I/O Impedance Levels* Feedback Topologies *Global and Local Feedback* *Dual Loop Feedback* Circuit Examples	Chapter 4 Chapter 5 Chapter 6 Lecture Aid 5 Lecture Aid 10
9	**10/24/2012**	***MIDTERM EXAMINATION*** ***DESIGN PROJECT ASSIGMENT***	***Open Notes & Book***
11	11/05/2012	CANONIC CELLS AT HIGH FREQUENCIES Common Source Amplifier *I/O Gain Frequency Response* *I/O Impedance Frequency Responses* *Active Loads* Common Drain Amplifier *I/O Gain Frequency Response* *I/O Impedance Frequency Responses* *Active Loads* Common Gate Amplifier *Low Frequency Characteristics* *High Frequency Properties* Transconductor Amplifiers	Chapter 7 Chapter 8 Lecture Aid 6 *(Cursory Review Only Is Given In Class)*
11, 12	11/05/2012 11/12/2012	BROADBAND AND RF AMPLIFIERS Pole Dominance Degenerative RC Broadbanding Response Peaking *Shunt Peaking* *Series Peaking* *Series-Shunt Peaking* Feedback Broadbanding Narrowband Tuning *Common Source RF* *Active Gate Impedance Compensation* *Frequency Response*	Chapter 9 Lecture Aid 7 Course Notes 4 Course Notes 5
13, 14, 15	11/19/2012 11/26/2012 12/03/2012	ELECTRICAL NOISE Noise Analysis Strategies *Time Domain Representation* *Frequency Domain Representation*	Lecture Aid 11 Tech. Reports

WEEK	WEEK OF	LECTURE TOPIC	READINGS
		Two-Port Network Models	
		Network Cascades	
		Noise In Devices	Tech. Reports
13, 14, 15	11/19/2012	*Johnson(Thermal) Noise*	
	11/26/2012	*Shot Noise*	
	12/03/2012	*Flicker Noise*	
		Noise In Subthreshold MOS	Tech. Reports
		Noise In Analog Canonic Cells	Tech. Reports
		Common Drain Amplifier	
		Source Follower	
		Common Gate Amplifier	
	12/17/2012 Last Class, 12/05/2012	***FINAL EXAMINATION (11:00AM –1:00 PM)***	***Open Notes, Open Book***

Dr. John Choma,
Professor of Electrical Engineering
Ming Hsieh Department of Electrical Engineering
01 August 2012

cc. Prof. E-S. Kim, Department Chair
Dr. Edward Maby, Associate Department Chair
Uldric Antao, Teaching Assistant
EE 536a–Website (www.jcatsc.com)