Department of Electrical Engineering
University of Southern California
EE 599 — Network Processor Programming and Design

Instructor: Young H. Cho, Research Assistant Professor
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Office hours: Tuesdays, Thursdays 2-3pm

TA: Siddharth Bhargav
Office hours: TBA

Course Web Page: https://education.deterlab.net/course/view.php?id=14
The web page will contain course announcements, laboratory assignment and relevant handouts.

Lecture times and dates: 12:30-1:50pm Tuesdays, Thursdays

Classroom Location: SGM (Seeley G. Mudd) 226

Course Objectives: Understand network processor architecture, applications, and other relevant issues. Program network processor and test under realistic network environment. Design and deploy custom network processor.

Pre-requisite: None.
Recommended Courses: EE450 and EE457
Other Requirements: experience in C programming and some understanding of hardware description languages

Grading:
5% Class participation
15% Reading assignments
40% Laboratory assignments
10% Final Presentation
30% Final Project
Final grades will be assigned by a combination of student score and the discretion of the instructor.

Preparation for classes:

- Students will be using Linux based system through the course. It is strongly recommended that the students become familiar with its navigation and use.
- Some of the laboratory assignments will require the use of C/C++ under Linux environment. It is recommended that students become familiar with the language and typical development environment.
- It is recommended that the students become familiar with some form of hardware description languages.

Grading policies:

- **Late Policy**: No late assignments will be accepted unless the instructor extends the due date. A late assignment results in a zero grade.

- **Grade Adjustment**: If you dispute any scoring of a problem on an exam or homework set, you have one week from the date that the graded paper is returned to request a change in the grade. After this time, no further alterations will be considered. All requests for a change in grade must be submitted in writing to me.
- **Changes/Information**: The student is responsible for all assignments, changes of assignments, announcements, lecture notes etc. All such changes should be posted on the course web-site.
- **Other**: As per university guidelines published in SCampus, the academic integrity policy will be upheld.

Statement for Students with Disabilities

Any student requesting academic accommodations based on a disability is required to register with Disability Services and Programs (DSP) each semester. A letter of verification for approved accommodations can be obtained from DSP. Please be sure the letter is delivered to me (or to TA) as early in the semester as possible. DSP is located in STU 301 and is open 8:30 a.m.–5:00 p.m., Monday through Friday. The phone number for DSP is (213) 740-0776.

Statement on Academic Integrity

USC seeks to maintain an optimal learning environment. General principles of academic honesty include the concept of respect for the intellectual property of others, the expectation that individual work will be submitted unless otherwise allowed by an instructor, and the obligations both to protect one's own academic work from misuse by others as well as to avoid using another's work as one's own. All students are expected to understand and abide by these principles. Scampus, the Student Guidebook, contains the Student Conduct Code in Section 11.00, while the recommended sanctions are located in Appendix A:http://www.usc.edu/dept/publications/SCAMPUS/gov/. Students will be referred to the Office of Student Judicial Affairs and Community Standards for further review, should there be any suspicion of academic dishonesty. The Review process can be found at: http://www.usc.edu/student-affairs/SJACS/.

Syllabus:

The course will be driven mainly by the lecture materials and assigned reading materials (key publications in the field).

Lecture Week	Topic
1	Introduction to Network Processing
2	Networking Basics
3	Network Appliances
4	Programmable Network Appliances
5	Hardware Accelerated Networking
6	Introduction to Network Processors
7	NetThreads Network Processor
8	FPGA/NetFPGA Architecture
9	NetFPGA Programming
10	Digital Logic and System Design Review
11	Computer Architecture Review
12	Extended Instruction Set Architecture
13	Integration of Network Controller with Processor
14	Application Specific Hardware Acceleration
15	Application: Network Intrusion Detection Systems

Laboratory #	Topic
1	DETER Tutorial (week 1)
2	Advanced DETER Tutorial (week 1)
3	Network performance measurement and tuning (week 2)
4	Xilinx ISE/Verilog Tutorials (week 2-3)
5	Mini Network Intrusion Detection System (week 4-5)
6	Custom Processor Design (week 6-7)
7	Special Network FIFO Design (week 8)
8	Single Core Network Processor Integration (week 9-10)
9	Final Project (week 10-15)

Course Reading List

1. B. Leiner, et al., "The DARPA Internet Protocol Suite", INFOCOM 85, Washington, D. C., March 1985.
2. T. Narten, "Internet Routing", ACM SigCom 89.
3. S. J. Lee, P. Sharma, S. Banerjee, S. Basu, and R. Fonseca, “Measuring bandwidth between planetlab nodes,” Passive and Active Network Measurement, p. 292–305, 2005.
4. L. White, et al, "An Integrated Experimental Environment for Distributed Systems and Networks", OSDI 2002, December 2002.

5 DETER team, "Cyber defense technology networking and evaluation", In Communications of the ACM, Special issue on Emerging Technologies for Homeland Security, Vol. 47, Issue 3, pp 58-61, March 2004.
6 G. Watson, "NetFPGA: A Tool for Network Research and Education", 2nd Workshop on Architecture Research using FPGA Platforms (WARFP) February, 2006.
7 C. Seitz, et al, "Myrinet: A gigabit-per-second local area network", IEEE MICRO Feb 1995.
8 P. Crowley, M. E. Fluczynski, J. L. Baer, and B. N. Bershad, “Characterizing processor architectures for programmable network interfaces,” in Proceedings of the 14th international conference on Supercomputing, 2000, p. 54–65.
9 M. Labrecque, J. G. Steffan, G. Salmon, M. Ghobadi, and Y. Ganjali, “NetThreads Routing Edition: Programming NetFPGA with Threaded Software.” NetFPGA Developers’ Workshop, 2009.
10 M. Labrecque, J. G. Steffan, G. Salmon, M. Ghobadi, and Y. Ganjali, “NetThreads: Programming NetFPGA with threaded software,” NetFPGA Developers’ Workshop, 2009.
11 A. Goodney, S. Narayan, V. Bhandwalkar, and Y. H. Cho, "Pattern Based Packet Filtering using NetFPGA in DETER Infrastructure," First Asia NetFPGA Developers' Workshop, Daejeon, Korea, June 2010.
12 Moscola, J. et al., "Reconfigurable Content-based Router Using Hardware-Accelerated Language Parser", ACM Transaction on Design Automation of Electronic Systems on Demonstrable Software Systems and Hardware Platforms, Volume 13, Number 2, April 2008.
13 M. Adiletta, M. Rosenbluth, D. Bernstein, G. Wolrich, and H. Wilkinson, “The next generation of Intel IXP network processors,” Intel technology journal, vol. 6, no. 3, p. 6–18, 2002.
14 N. McKeown et al., “OpenFlow: enabling innovation in campus networks,” ACM SIGCOMM Computer Communication Review, vol. 38, no. 2, p. 69–74, 2008.