University of Southern California
Viterbi School of Engineering
Ming Hsieh Department of Electrical Engineering

EE 479 - Analog and Non-linear Integrated Circuit Design

Instructor: Ali Zadeh
Email: prof.zadeh@yahoo.com
Lecture: Tuesday 6:40 - 9:20pm
Discussion: Friday 2:00 – 2:50pm
Term: Fall 2011
Office Hour: 9:20 - 10:20pm
Pre-requisite: EE 348L
Office location: Powel Hall 532

Pre-requisite:

- Linear-Time Invariant (LTI) systems, Signals and Systems, time domain (t-domain) vs. complex frequency domain (s-domain) analysis, RLC networks, Laplace transform, KCL, KVL, basic Diode, BJT, and MOS operations and circuits, basic feedback block diagram.
- Study Frequency Domain vs. Time domain will be covered in the discussion section.

Required Text Book:

- P. R. Gray, P. J. Hurst, S. H. Lewis, & R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5-th Edition, John Wiley & Sons, Inc., New York, 2009.

Reference Text Books:

- R. Jacob Baker, *CMOS Circuit Design, Layout, and Simulation*, 3rd Edition, IEEE Press, 2010.
- P. E. Allen & D. R. Holberg, *CMOS Analog Circuit Design*, 2nd Ed, Oxford University press, 2002.
- B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw Hill, 2001.
- D. A. Johns & K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, New York, 1997.

Class Website: All lecture notes, assignments and announcements will be posted on DEN. Please check EE 479 Class Website on DEN once a day.

Course Goal:

- EE479 covers analysis and design of Analog and Non-Linear Integrated Circuits. The course consists of two sides of dealing with Analog Integrated circuits: (a) Analyzing a given Analog Integrated circuits through homework exercises and exams. (2) Designing Analog integrated circuit is accomplished by a major final project.

- The emphasis of the course material will be on CMOS analog circuits such as current sources, active load, bias current and voltages, differential pairs, frequency response, feedback amplifiers, output stages, noise behavior, Miller compensation, one-stage and two stage CMOS operational amplifier, folded-cascode, telescopic, operational transconductance amplifier (OTA), high-performance, low-voltage, and high-speed CMOS operational amplifier. We may cover band-gap circuits and voltage references. Finally, we will cover material on the Analog non-linear integrated circuits such as large signal analysis, distortion, and crystal oscillators.

Grade: Final course grade is based on the following formula:

Homework Assignments	=	25%
Midterm I Exam	=	25%
Midterm II Exam	=	25%
Class Project	=	25%
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Total	=	100%

Instructor's Background:

I am a part-time faculty in the Electrical Engineering department. I have worked in Semiconductor and Medical companies since 1982 and designed many Analog and Mixed-Signal Integrated circuits: Switched-Capacitor Filters, Analog-Digital Interface Integrated Circuits, Micro-power Biomedical Data-Converter Integrated Circuits and Systems, and CMOS Image sensors.

Exams

There will two Midterm exams: The dates of exams will be announced in the class schedule. The second Midterm is NOT cumulative. It covers only the material after the first midterm.

Exams will be closed book. Students can bring one 8.5" x 11" page (both sides of the sheet) of notes for the midterms. Paper for exams will be supplied. Just bring a pencil, eraser, and a calculator. You must show how you have derived the answers fully in order to receive full credit.

Homework Assignments

There will be six homework assignments given during the semester. Homework assignments will be given through the class web-site and are due by the announcements. If you cannot make it to the lecture, have a friend to turn in your homework for you.

Homework Policies:

- Up to 10 points of your homework grade is based on following these policies.
- Your homework must be a professional quality work.
- I expect you to spend time on doing your homework assignments.
- Use only standard 8.5 in x 11 in papers.
- Use only one-side of each page.
- Put stables on the upper-left corner.
- Write nicely, large, neatly and legibly.
- Put each schematic diagram and/or simulation results in a separate page.
- Add a cover page with your name according to USC records: ***Last Name, First Name.***
- Each person does his/her homework individually.
- Copying homework from each other is considered cheating.
- Turn in your homework in the classroom at the beginning of the lecture.
- Late homework and E-mail homework will NOT be accepted.

Cadence Spectre Simulation:

- We will be using Cadence Analog Artist for simulations of our circuits, homework and project. In this class we will be using ***65nm CMOS process technology from IBM.***
- We will use state-of-the-art BSIM4 model file for IBM-65nm technology for simulations.
- In the Homework assignments and the Project assignment, we will be using Cadence to simulate, verify and optimize the circuits. In this class, we will NOT do any IC layout.
- The IC simulation software used in the EE-479 class is called ***SPECTRE***.
- Spectre is the Cadence version of widely used circuit simulator SPICE. Nowadays, the Cadence (Spectre) is the semiconductor and electronic industry standard simulation tool. This class will prepare students for the industry type of work. The same software tool is also used in other classes such as EE-477L, EE 448L, EE-536A & B, EE-577A & B.
- You will have help from your TA to get setup and run simulations.
- There are many websites that also can help you using Cadence in simulations.

Class Project

One of the main purposes of the course is for student to have hands-on experience in designing a major CMOS Operational Amplifier integrated circuit using Cadence.

1. Your project report must be professional quality work, done in the MS-words, Handwritten project will NOT be accepted.
2. Use: Insert Object > Microsoft Equation 3.0, to make formula and equations for your project report.
3. Use: plot > post-script in Cadence to make graphs and plots > copy in your report.
4. Either one or two persons can work on the same project. Because of the amount of work, I do recommend two people.

The performance specification of the project operational amplifier is in Table 1. This opamp is an embedded operational amplifier and it is designed to be a part of a larger high-speed Mixed-Signal Integrated circuit or system.

The class project is graded based on:

Organization and Project Report:	10%
Analysis and Hand Calculations:	10%
Circuit Design Innovation:	10%
Circuits /Test Circuit Diagrams:	10%
Graphs and Waveforms:	10%
Specification Performance:	50%
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Total	**100%**

Parameter Description	Desired	Achieved	Value	Priority
Power Supply Voltage (Vdd)	2.0	2.0	V	--------
Temperature (Room)	25	25	°C	--------
IBM65nm Process Corner	Typical	Typical	-----	--------
Output Load Capacitor	1	1	pF	--------
Opamp Open Loop DC Gain (Avo)	> 100		dB	1
Opamp Unity Gain-Bandwidth Product (GBW)	> 1GHz		MHz	1
Phase Margin	> 65		Degree	1
Positive Settling Time (0.01% of 1V input step)	< 5		ns	1
Negative Settling Time (0.01% of 1V input step)	< 5		ns	1
Supply Current Consumption (Idd)	< 25		mA	2
Power Consumption (Vdd X Idd)	< 50		mW	2
Positive Slew Rate (SR+)	> 1		V/ns	2
Negative Slew Rate (SR-)	> 1		V/ns	2
Input Common-Mode Range (ICMR)	> 1	Vin1-to-Vin2 =?	V	2
Analog Signal Ground (reference) Voltage	-----	?	V	2
Positive Power Supply Rejection Ratio (at 100Hz)	> 60		dB	3
Negative Power Supply Rejection Ratio (at 100Hz)	> 60		dB	3
Common Mode Rejection Ratio (at 100Hz)	> 60		dB	3

Table 1. CMOS Operational Amplifier Specification for the Class project.

Achieving all these specifications simultaneously will be challenging. Several papers and patents will be provided at the end of the semester to give you some ideas how to push the performance of your circuit. First try to achieve the minimum possible performance. Then, improve the opamp performance if you have additional time.

EE 479 Weekly Schedule, Fall 2011

Week	First Half	Second Half	Readings
(1)	Introduction: • Syllabus • Analog vs. Digital	Frequency vs. Time Domain: • Linear-Time Invariant (LTI) system • First order & Second order networks	**Chapter 1**
(2)	PN Junction., MOS Device: • Ohmic (Triode) Region • Saturation (Active) Region	MOS Device in Saturation Region: • AC Small-Signal Equivalent • Transconductace, Output Resistance	**Chapter 2**
(3)	MOS Device 2nd order effects: • Channel Length Modulation (λ) • Body Effect (γ, χ)	MOS Device: • High-frequency Model • Gate & Junction Capacitances	**Chapter 3**
(4)	Amplifier Configurations: • Common Source (CS) • Common Gate (CG) • Source Follower (SF)	Multi-Transistor Amplifier: • Cascade Configuration • Cascode Configuration • Gain enhancements	**Chapter 3**
(5)	Differential Pair Amplifiers: • Differential Mode • Common Mode	Current Mirrors: • Cascode • Low-voltage Cascode	**Chapter 4**
(6)	Differential Pair Amplifiers: • Active Load	References: • Current & Voltage References	**Chapter 4**
(7)	References: • Supply Independent Bias Current • PTAT Current Source	Opamp Specifications: • Single-Ended output • CMRR, PSRR+, PSRR-, ICMR	**Chapter 6**
(8)	Midterm I Review **Midterm I : Chapters: 1, 2, 3, 4**	**Midterm I Exam** **8:00 pm – 9:20 pm**	
(9)	Opamp Topologies: • Telescopic, Folded-Cascode, OTA	Opamp Topologies: • Telescopic, Folded-Cascode, OTA	**Chapter 6**
(10)	Amplifier Frequency Response: • CS, CG, SF Configurations	Amplifier Frequency Response: • CS, CG, SF Configurations	**Chapter 7**
(11)	Analysis of Feedback System • Return Ratio • Loop-Gain	Amplifier feedback: • First Order Model. • Gain-Bandwidth Trade-off	**Chapter 8**
(12)	Amplifier feedback: • Second Order Model • Frequency vs. Transient Response	Amplifier feedback: • Second Order Model • Frequency vs. Transient Response	**Chapter 9**
(13)	Two-Stage Operational Amplifier: • Miller Compensation	Two-Stage Operational Amplifier: • Frequency vs. Transient Response	**Chapter 9**
(14)	Non-Linear Analog Circuits: • MOS Distortion Analysis	Non-Linear Analog Circuits: • MOS Crystal's oscillator.	**Notes**
(15)	Midterm II Review **Midterm II: Chapters: 6, 7, 8, 9**	Project Review, Class Evaluation • Design of Two-Stage CMOS Opamp	**Notes**
(16)	----------	**Midterm II Exam** **According to University Schedule**	----------
(17)	----------	**Final Project Report** **Due Date:**	---------