EE 457 Syllabus Handout Fall 2010 Instructor: Gandhi Puvvada

Computer Systems Organization

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1. Abstract: This course covers computer organization and design. It provides CS/CE/EE students a substantial understanding of a CPU at its logic design level. Design of the control unit and the data path unit of a simple multi-clock-cycle CPU and a pipelined CPU is covered in detail. Hardware support for exceptions, dynamic scheduling of instructions (Tomasulo algorithm to execute instructions in an out-of-order fashion), and branch prediction are also discussed. Computer arithmetic and memory hierarchies (cache, main memory, virtual memory) are also covered. Hardware-software interface is discussed. Students design in Verilog and use ModelSim simulator to verify their design/simulation exercises.

At the end of the course, students are expected to feel confident to perform logic design of a CPU or any hardware system utilizing pipelining and other RTL techniques and proceed to graduate courses in computer architecture or general hardware design.

2. Course administration

a) Course prerequisites: EE201L Introduction to Digital Circuits and EE357 Basic Organization of Computer Systems are the *necessary* prerequisites. Undergraduate students without these prerequisites will not be able to do this course. Graduate students are expected to have taken a logic design course and a course covering some assembly language in their undergraduate course work before taking this course.

b) Classes: http://www.usc.edu/academics/classes/term_20103/classes/ee.html

Lec	30604R	05:00-06:20pm MW	Puvvada	ZHS252
Lec	30568R	12:30-01:50pm TTh	Puvvada	ZHS252
Lec	30567R	03:30-04:50pm TTh	Puvvada	OHE132
Lec	014-30572R	03:30-04:50pm TTh	Puvvada	Off Campus

Dis	30569R	01:00-01:50pm W	TA	OHE132
Dis	014-30573R	01:00-01:50pm W	TA	Off Campus
Dis	30605R	12:00-12:50pm F	TA	SLH102
Dis	30570R	03:00-03:50pm F	TA	SLH100

Discussion class is *not optional*. The lab assignments are primarily discussed during the discussion class. Important additional material may be covered in the discussion class.

c) Examinations: **No make up exams.**

One quiz (~10%) and one midterm (~20%) and the final exam (~30%)

The "Quiz" slot (Qz 10:00 – 12:00 pm Friday)
We will utilize this slot only twice in the whole semester to conduct a quiz and a midterm.
So it is ok to have schedule conflict with the quiz slot
provided you agree to make yourself available for these two occasions.

Quiz (~10%): Friday Oct. 1, 2010 10:00 AM - 12:00 PM PST (the quiz slot). Exam Hall: _____
Please note that the exam may be 2H 30Min up to 12:30PM. I want you all to keep this 30 min.
extra time available for possible extensions of exam time.

Midterm (~20%): Friday Nov. 5, 2010 10:00 AM - 12:30 PM PST (the quiz slot, extended). Exam Hall:
_____
Please note that the exam will most likely be 2H 30Min up to 12:30PM. I want you all to keep this 30 min.
extra time available for possible extensions of exam time.

Nov 12	Last day to drop a class with a mark of "W"

http://www.usc.edu/academics/classes/term_20103/calendar.html

Final Exam (~30%): Friday, Dec 10, 2010 8:00-10:30 a.m. PST Exam Hall _____ (TBA)

Please note that the exam will most likely be 2H 30Min up to 10:30AM. I want you all to keep this 30 min.
extra time available for possible extensions of exam time.
Hope none of you have any conflict with this extra 30 min.
Note: EE457 Final Exam is as per the Exceptions Schedule posted at the bottom of:
http://www.usc.edu/academics/classes/term_20103/finals.html

d) Grading Policy:

Weights of course components:
Quiz: **~10%**, Midterm Exam **~20%** No make-up exams.
Homeworks **10% to 15%** (penalty for late submission: up to 5% per day if solution has not been distributed).
*Design projects** **25% to 35%** (penalty for late submission: 2% per day up to 7 days, 3% per day after 7 days).
Final exam **~30%** No make-up exam.

* *We will be using* Modelsim Verilog design entry and simulation tools *to do a number of design exercises.*

e) Academic Accommodations:

Any student requiring academic accommodations based on a disability is required to register with
Center for Academic Support and Disability Services and Programs (CAS & DSP) each semester. A letter of verification for approved accommodations can be obtained from (CAS & DSP).
Please be sure the letter is delivered to me as early in the semester as possible
(no less than 2 weeks before an exam).
The CAS & DSP office is located in STU 301 and is open 8:30 a.m. - 5:00 p.m., Monday through Friday.
Their phone number is (213) 740-0776.
http://sait.usc.edu/academicsupport/centerprograms/dsp/home_index.html

f) Miscellaneous administrative matters:

Lecture class attendance, penalty for absence, and minimum required performance:

If you miss more than 2 lecture meetings, you will start noticing that you are falling behind.

If you miss more than 5 lecture meetings, you may as well drop the course.
It is a design course requiring continuity in your learning process. So, please attend every lecture meeting.
The following penalty rule is based on a total of 28 attendance markings. This rule does not apply to remote students, as I cannot monitor their attendance. They are allowed to watch the lecture in the evening/late night.

Penalty for lecture absence: 1% for 5th, 6th, 7th, 2% for 8th, 9th, and 4% for 10th and after.
Penalty for discussion absence: 0.5% for 3rd, 4th, 5th, 6th, 1% for 7th and after.

Homeworks shall be done individually. Design and simulation projects can be performed either individually or in teams of two students (2 per team). But occasionally, even design labs may be assigned as individual assignments.
Teams shall submit one set of Verilog code online and waveforms in hard copy as stated in the assignment. **However justifications/explanations, state diagrams, and answers to questions at the end of the lab assignment**
shall be prepared individually. *Copying is different from discussing ideas with other students.*
You are encouraged to share your thoughts on homework, design projects, and design project reports with others. Absolutely no copying. If you turn in some work and you cannot explain your own work, then we infer that you copied. Do NOT try to copy design files. We have ways to find if a design/simulation project has been copied. If you submit a **non-working design/lab** and do not write on the top of it in **BIG** letters that it is NOT WORKING (and further do not inform the instructor, the TAs and the lab graders through email), we will treat it as an attempt to cheat. This is very important. Try not submitting a non-working lab as we give very little credit for a non-working lab. We are here to help you and guide you in your debugging.

Academic dishonesty cases will be dealt with severely. You must have gone through the short presentation on Academic Integrity at USC at Academic Integrity Tutorial and Quiz - Fall 2010 posted on your DEN blackboard.
A tutorial is also posted at http://usccollege.na4.acrobat.com/academicintegrity. Another important resource is the
Student Judicial Affairs and Community Standards (SJACS) Website
http://www.usc.edu/student-affairs/SJACS/index.html . You may want to visit
http://www.usc.edu/student-affairs/SJACS/pages/students/community_standards.html
University policy requires that all academic integrity violations must be reported to Student Judicial Affairs and Community Standards (SJACS).

We will try to make the assignments due on times far from the class time.
This is to make sure that students do not miss classes to complete the assignments.

Please check your email regularly. Also visit the DEN blackboard (http://www.uscden.net/) regularly.

g) Instructor: Gandhi Puvvada (email: gandhi@usc.edu)
Office: EEB238 Phone: (213) 740-4461
Office hours: http://www-classes.usc.edu/engr/ee-s/457/Gandhi_Office_Hours.pdf
Home phone number: (310) 839-3933 (up to 10:00PM any day including weekends and holidays)

Students are encouraged to discuss any difficulties they are facing in this course with any of us (TAs, Mentors, graders or myself).

h) Teaching Assistants:

EE457 TA -- Jonathan Joshi <jjoshi@usc.edu>
EE457 TA -- Prasanjeet Das prasanjd@usc.edu
EE457 TA -- Mehrtash Manoochehri <mmanooch@usc.edu>
EE457 TA -- Sabyasachi Ghosh <sabyasag@usc.edu>

Office Hours: Look under staff information on the blackboard.
Please make appointments with the TA(s)/Mentor(s) through email for additional help.

The TAs conduct the discussion sessions. The TAs and the Mentors are primarily responsible for class material, design/simulation projects, end-of-the-lab questions, and homeworks.
For any difficulty with ModelSim or with your simulation exercises, you should first try to approach the TA/Mentor. If none is not available, you should then contact the instructor. In any case do not delay getting help.

Homework grader can help on homeworks and the lab grader can help on the design/simulation projects and end-of-the-lab questions.
For help on lecture material, it is best to see the instructor.

i) Graders:
TBA
Office Hours: Look under staff information on the blackboard.

3. Design/simulation projects schedule:

Approximately one lab (or one part of one lab) will be assigned every week starting from the second week.

The labs make up the **25%** to **35%** of your course credit. The points indicated are tentative. We may decide to assign quite different points/weights to individual labs. We may also replace some old labs with new labs but the total weight of labs makes up **25%** to **35%** of your course credit. We may also decide to remove some existing labs and introduce new labs.

o) Introduction to Verilog HDL entry and simulation in Modelsim

1) Max. Min. finder State Machine Design Lab #1 Part #1 and #2, Part #3 (M1 & M2), Part 4 (200 points)

2) RTL Exercises (to be developed) (200 points)

3) Design of a 32-bit ALU Lab #3 (100 points)
3a) Design of a combinational divider (30 points)
3b) Design of a special divider (100 points)

4) Multi-cycle CPU Design Lab #4 Part #4 (100 points)

5) Pipelined Ripple Carry Adder Design Lab #5 (cancelled)

6) Design of a Pipelined CPU (Revised in Summer 2010) Lab #6 Part #2, Part #5 and #4
(parts 2: 200 points, part 5: 200 points, part 4: 100 points)

7) Design of a 3-element adder Lab #7 Part #1, #2, #3, #4 (Part 1: 150 points, part 2: 100 points, part 3: 100 points, part 4: 100 points)

8) New labs (Yet to be developed)
Cache (150 points)
CLA, Multiplier using a linear cascade of CSAs (150 points)

4. Readings: The required readings are class notes and sections of the textbook. Please make it a practice to read regularly. It is important to clarify any items that are not clear in that week itself.
Students, who postpone reading, gradually drift away from the rest of the class and eventually perform very poorly on the exams and design/simulation projects.

Primary References:

Class Notes (required): Please buy from the university (USC) bookstore.
Remote can place their orders online for the class notes and other items at the following website.
http://www.uscbookstore.com/site_distance_education.asp?mscssid=80004351255E4DF69F772DD0F1AD9E9A
If there is any problem, please call (213) 740-TEXT and also let me know if the problem cannot be resolved.

Lab Manual: Since the labs are being revised (and being converted to Verilog), the labs will be distributed through BB posting.

Textbook/Verilog Guide:
1. Computer Organization & Design - The Hardware and Software Interface 4th edition
By D. A. Patterson (Berkeley) and J. L. Hennesy (Stanford)
Please buy from the university (USC) bookstore or any place (such as online bookstores).
http://www.elsevierdirect.com/product.jsp?isbn=9780123744937
If you have second edition of the textbook, or the 3rd edition but not the 4th editon, that is fine too.
I do not have any experience with the following discount vendor, but if it works, it is good!
http://www.cheapesttextbooks.com/
2. The Verilog 2001 Reference Guide by Esperan (Cadence)
You need this for your Verilog-based design/simulation labs. **You can use it in the EE457 exams**.
Esperan (Cadence) does not sell it to individuals. USC Bookstores does not have it.
We are making alternative arrangements for you to buy a copy of the same from the EE department.

Secondary References (Do not buy these):

1. EE101 and EE201L Textbook: Digital Design Principles and Practices By John F. Wakerly
2. EE357 Textbook: Computer Organization by Hamacher
3. Advanced Computer Architecture with Parallel Programming By Kai Hwang
4. Computer Architecture - A Quantitative Approach By D. A. Patterson and J. L. Hennessy
5. Computer Arithmetic Algorithms By Israel Koren

5. Tentative Course Schedule (for a 14-week (28 lecture) regular semester):

# of lectures	Lecture	Item	Comment	Homework /Lab
2	1, 2	Intro to course review of prerequisite material	Review datapath and control unit design, Compare and contrast: state diagram vs. flow-chart	HW & Lab

1	3	Performance		HW
3	4, 5, 6	MIPs ISA, SLT, SLTU instructions	Review overflow detection in unsigned and signed arithmetic and also cover word addresses in a byte addressable processor	HW
2	7, 8	Single Cycle CPU	Datapath and control design	HW
4	9, 10, 11, 12	5-stage pipeline	Cover data dependency solutions (Compiler solution, HDU & FU), and branch implementations (late branch vs. early branch), branch delay slots. Also cover exceptions.	HW & Lab
5	13, 14, 15, 16, 17	Cache and Virtual memory	Mapping techniques, CPU address division into fields and connect address to Cache Data RAMs, Cache Tag RAMs, TLBs, and interleaved main memory. Multi-level page table, PTBR, principle of inclusion.	Cache HW Virtual Memory HW Lab?
1	18	**Midterm**		
2	19, 20	Arithmetic	Carry-Look-ahead adder, and Wallace-Tree Multiplier using CSAs	HW
1	21	Exceptions	Exception PC and Cause register	
2	22, 23	Out of order execution and Tomasulo algorithm	WAR and WAW hazards in OoO execution, IFQ (Instruction prefetch queue), dispatch unit, issue queues, issue unit, CDB, ROB	
1	24	Brach Prediction	1-bit and 2-bit predictors, BPB, BTB	
1	25	Speculative execution	ROB, exception handling, handling mispredicts	
1	26	CMP	Thread-level parallelism	
1	27	Non-linear pipelines		HW
1	28	Cache Coherency	Snoopy protocol, Write through vs. write-back, MESI	

********** **Final Examination Comprehensive.** **********