EE 505 – Analog, Mixed Signal, and Radio-Frequency Integrated Circuit Tape-Out

University of Southern California

Ming Hsieh Department of Electrical Engineering

Fall 2016 Semester

Course Number: EE 505
Course Title: Analog, Mixed Signal, and Radio-Frequency Integrated Circuit Tape-Out
Units: 3
Class Schedule: Tuesday and Thursday, 3:30 pm – 4:50 pm
Class Room: VKC 109
Instructor: SungWon Chung (chungsun@usc.edu)
Office Hours: TBD
Teaching Assistant: TBD
Office Hours: TBD
Prerequisite: EE536a or EE479. Otherwise, an equivalent with permission.
Supplementary Texts:
Course Website: http://blackboard.usc.edu
Lecture notes, assignments, and announcements will be posted.
Catalog Description: Complete systematic tape-out flow including schematic design, simulation, layout, and post-layout verification of analog, mixed-signal, or radio-frequency integrated circuits.
**Course Description:**
EE 505 is a graduate course designed to provide a systematic view of the integrated circuit tape-out process. The course discusses the layout techniques as well as several critical concepts needed for realization of complex systems-on-a-chip. Each student will complete the design, simulation, and tape-out of an analog, mixed-signal, or radio-frequency building block or system to satisfy a predetermined set of specifications. Graduate students who master EE 536ab and EE 505 would be competitive for entry-level positions in integrated circuit design.

**Grading:**
- Homework  20%
- Quiz 30%
- Design Project 50%

**Homework Policy:**
Late homework and e-mail homework will not be accepted. Each person does one own homework individually. Although it is encouraged to discuss with peer students on how to approach the problem, solution write-ups must be independently done. Use standard letter papers (8.5in x 11.0in). Use only one-side of each paper and put stables on the upper left corner. Make sure numbers, units, and labels on simulation plots are clearly visible. Turn in your homework in the classroom by the end of the lecture. Each homework takes 5% in grading. The homework with the lowest score is omitted in the final grading.

**Design Project:**
Design project is a major component of EE 505. Each student will go through a complete analog/mixed signal tape-out flow including design, simulations, layout, and post-layout verification using a commercial foundry Process Design Kit (PDK) and Cadence full-custom circuit simulation and layout tools. Examples of integrated circuits for the design project include wireless communication radio-frequency front-end, analog/mixed-signal back-end, high performance data converters (ADC and DAC), frequency synthesizers, and power management systems. Students will present their progress in four design review presentations. Selected students with innovative and complete design may get a chance to fabricate and measure their chips in the following two semesters, leading to a peer-reviewed journal publication.

The design project (total 50%) will be graded as the following:
- Schematic Design Review I: 5%
- Schematic Design Review II: 10%
- Layout Design Review I: 5%
- Layout Design Review II: 10%
- Interim Design Project Report: 5%
- Final Design Project Report: 15%
**Tentative Weekly Lecture Schedule**

<table>
<thead>
<tr>
<th>Week</th>
<th>Date</th>
<th>Topic</th>
<th>Assignments</th>
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<tbody>
<tr>
<td>1</td>
<td>8/23</td>
<td>IC design flow; Silicon vs III-V processes; Modern technologies (high-k, FD-SOI, FinFet, Heterogeneous, …)</td>
<td>Design project issued HW #1 assigned (initial design method)</td>
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<tr>
<td>2</td>
<td>8/30</td>
<td>MOSFET; Moore’s law; Amdhal’s law; Rent’s rule; Dennard scaling; Effects of scaling; Review of circuit building blocks</td>
<td>HW #1 due HW #2 issued (variation)</td>
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<td>3</td>
<td>9/6</td>
<td>Variations – Passive elements; Active elements; Impact of process variations; Monte Carlo simulations</td>
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<tr>
<td>4</td>
<td>9/13</td>
<td>Mismatch – Phenomenology; Modeling; Mitigation strategies; Calibration; Simulation methods for mismatch evaluation</td>
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<tr>
<td>5</td>
<td>9/20</td>
<td>Design Project Review I: Block-Level Circuit Design</td>
<td>HW #2 due HW #3 issued (mismatch)</td>
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<tr>
<td>6*</td>
<td>9/27</td>
<td>Supply regulation – Bypass design; Ground techniques; Layout floor-planning; Parasitic extraction</td>
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<td>7</td>
<td>10/4</td>
<td>Electro-Static Discharge – Physics; Models; Mitigation strategies, Manufacturing issues – Latch-up; Antenna; Bond-Pad; Seal-Ring</td>
<td>HW #3 due HW #4 issued (physical layout)</td>
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<td>8</td>
<td>10/11</td>
<td>Design Project Review II: System-Level Circuit Design</td>
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<tr>
<td>9</td>
<td>10/18</td>
<td>Electro-Magnetic Interference (EMI) – Mechanisms; Effects; Mitigation strategies</td>
<td>HW #4 due HW #5 issue (parasitic extraction)</td>
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<tr>
<td>10*</td>
<td>10/25</td>
<td>Aging &amp; reliability of MOSFET – Breakdown phenomena; Electro-migration; Pattern density; Thermal issues</td>
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<tr>
<td>11</td>
<td>11/1</td>
<td>High-Speed I/O Interface – Serial-link architecture; chip ID; e-Fuse; On-chip micro-controller</td>
<td>HW #5 due</td>
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<tr>
<td>12</td>
<td>11/8</td>
<td>Design Project Review III: Block-Level Layout</td>
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<tr>
<td>13</td>
<td>11/15</td>
<td>IC Test &amp; Packaging – Wirebonding; Flip-chip; Interposer; 3D packaging; HDI PCB</td>
<td>Interim design report due</td>
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<td>14</td>
<td>11/22</td>
<td>SoC Design Case Study – Guest speaker presentation</td>
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<td>15</td>
<td>11/29</td>
<td>Design Project Review IV: System-Level Layout</td>
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<td>12/1</td>
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<td>Design Project Final Design Report Due</td>
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Note: *Quiz in the beginning of the class
Statement on Academic Conduct and Support Systems

Academic Conduct

Plagiarism – presenting someone else’s ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in SCampus in Section 11, Behavior Violating University Standards https://scampus.usc.edu/1100-behavior-violating-university-standards-and-appropriate-sanctions/. Other forms of academic dishonesty are equally unacceptable. See additional information in SCampus and university policies on scientific misconduct, http://policy.usc.edu/scientific-misconduct/.

Discrimination, sexual assault, and harassment are not tolerated by the university. You are encouraged to report any incidents to the Office of Equity and Diversity http://equity.usc.edu/ or to the Department of Public Safety http://capsnet.usc.edu/department/department-public-safety/online-forms/contact-us. This is important for the safety whole USC community. Another member of the university community – such as a friend, classmate, advisor, or faculty member – can help initiate the report, or can initiate the report on behalf of another person. The Center for Women and Men http://www.usc.edu/student-affairs/cwm/ provides 24/7 confidential support, and the sexual assault resource center webpage sarc@usc.edu describes reporting options and other resources.

Support Systems

A number of USC’s schools provide support for students who need help with scholarly writing. Check with your advisor or program staff to find out more. Students whose primary language is not English should check with the American Language Institute http://dornsife.usc.edu/ali, which sponsors courses and workshops specifically for international graduate students. The Office of Disability Services and Programs http://sait.usc.edu/academicsupport/centerprograms/dsp/home_index.html provides certification for students with disabilities and helps arrange the relevant accommodations. If an officially declared emergency makes travel to campus infeasible, USC Emergency Information http://emergency.usc.edu/ will provide safety and other updates, including ways in which instruction will be continued by means of blackboard, teleconferencing, and other technology.