University of Southern California
Department of Electrical Engineering

EE 477L, MOS VLSI Circuit Design

Instructor: Ali Zadeh
Lecture: Friday 9:00 – 11:50 am
Lab Section: Two Lab sections
Pre-requisite: EE 327 or EE 338

Class Email: usc.ee477@yahoo.com
Classroom: OHE 100B
Office Hour: Friday 1:00 – 2:00 pm
Office location: Powel Hall, PHE # 532

Description:

This course provides an introduction to analysis and design of digital MOS VLSI circuits including area, delay and power minimization. The course explores the design aspects involved in the realization of CMOS integrated circuits from device up to the register level. The course includes the study of the MOS devices, logic cells, and critical interconnect and cell characteristics that determine the performance of VLSI circuits. Students will use CAD tools to develop efficient circuit layouts and verify designs. Laboratory assignments include design, layout, extraction, and simulation.

Textbook: *CMOS Digital Integrated Circuits*, Kang, Leblebici, and Kim, Mc Graw Hill, 4th-Edition, 2015.

Other References:

- *CMOS VLSI Design: A Circuits and Systems Perspective*, N. Weste and D. Harris, Addison-Wesley, 4th edition, 2011.
- *Analysis and Design of Digital Integrated Circuits*, Hodges, Jackson, and Saleh, McGraw-Hill, 3rd edition 2004
- *Digital Integrated Circuits: A Design Perspective*, J. Rabaey, Prentice Hall, 2nd edition, 2003.
- *CMOS IC Layout: Concepts, Methodologies and Tools*, D. Clein, 2000.

Class Website: https://blackboard.usc.edu/

- Lecture notes, assignments, class discussions, and announcements will be posted on Blackboard.
- Please check EE-477 Class Website on Blackboard once a day.

Grade Credit:

6 Homeworks	20%
Midterm 1	25%
Midterm 2	25%
3 Projects	30%
=========	=====
Total	100%

Instructor Background

I have been a part-time instructor in the Electrical Engineering Department since 2007. I have been a mixed-signal VLSI design Engineer all my professional career since 1982 for several companies: Harris Semiconductor, Siemens Corporation, Microsemi Corporation, Micron Technology, and St. Jude Medical. I am now a principal VLSI circuit design Engineer at Alfred Mann Foundation (AMF).

Exams

There will two Exams: a Midterm I and Midterm II (or Final Exam). The dates of exams will be announced in the class schedule. The Midterm II is NOT cumulative; it covers only the material after the Midterm I exam.

Exams will be closed book. You can bring one 8.5" x 11" page (both sides of the sheet) of notes for the each exam. Paper for exams will be supplied. Just bring a pencil, eraser, and a calculator. You must show how you have derived the answers fully in order to receive full credit.

Homework Assignments

There will be 6 homework assignments given during the semester. Homework assignments will be given through the class web-site and are due by the announcements. I will announce how we collect Homework assignments

Homework Policies:

1. Your homework should be a professional quality work.
   - Use only standard 8.5 in x 11 in papers.
   - Use only one-side of each page.
   - Put staples on the upper-left corner of your homework.
   - Write nicely, large, neatly and legibly.
   - Put each schematic diagram or simulation results in a separate page.
   - Cover page with your name according to USC records: Last Name, First Name.
2. Each person does his/her homework individually.
3. Copying homework and Lab Assignments from each other is considered cheating.
4. Turn in your homework in the discussion/lab time.
5. Late homework and E-mail homework will NOT be accepted.

Lab Assignments

There are three lab assignments, which collectively form a project. The lab/discussion section meets occasionally in the ITS computer classrooms, and sometimes in the assigned classroom.

About the Class:

Communication with the class is primarily through class meetings, email and backboard. Email is used to announce new postings to the class web site. All homework assignments, homework solutions, lab assignments, information about lab software, and study problems are posted on the web. If you are not receiving class email after about a week, you should contact the professor to make sure you are on the mailing list. **Be sure to keep your mail box clean and empty, so the class messages do not bounce back**. **You don't want to miss some material.**

The course syllabus contains reading assignments, as well as the outline of topics covered, and dates. You will get the most out of the class if you read the assignments before the lectures on each topic. Please note the date for the midterm examination. We will try to adhere to this date so you can plan your time.

Be sure to read the class Academic Integrity Policy posted on the class website. It contains important information on when it is permissible to collaborate with your classmates. Be sure you have the prerequisites for the class. If you are a graduate student, and did not have Electrical Engineering circuit courses as an undergraduate, please contact me. Also, if you need a certain grade in this class in order to graduate, please contact me immediately so we can work together to maximize your chances for success in this class.

Course Philosophy:

The course philosophy and focus of the class is on problem solving and design techniques. The class is a ***design*** class, although some of the material covered involves ***analysis***. It is more important to be able to reason about a given situation, rather than applying some "canned" memorized solution. The exams are open book, and understanding/application of basic principles is emphasized.

Course Workload:

Past students have stated that they found the workload to be about average. The lab assignments are very important and it is essential that you balance your time between this class and other classes so that you can complete the lab assignments. You can lose a letter grade or even two letter grades if you do not submit the labs.

Late Policy:

Late homework will have 10% deducted for every day late. Late homework will not be accepted after solutions are posted. Late labs will have 10% deducted per day, unless there is ITS problem or a problem with the lab software. It is your responsibility to inform me and the TAs if you are experiencing a software problem while performing the labs. Announcements are made at the beginning of class. Attending the lecture is extremely important as information may be provided that is not in the text.

Final Project:

The course Final project is usually the design, simulation, physical layout, and post-layout versifications of a practical industry-oriented VLSI circuit. We will cover this toward the end of the semester.

Tentative Weekly Schedule

Week	Subjects	Reading Assignments
1 ***Jan. 15***	Class Introduction. Introduction to CMOS Circuits, MOS Transistor Theory, Stick Diagrams, Transmission gates.	Chapter 1
2 ***Jan. 22***	CMOS Processing Technology and Fabrications, CMOS layout Design Rules.	Chapter 2
3 ***Jan. 29***	CMOS Physical Design, Euler Paths, Interconnections, chip layout Strategies	Chapter 7 ***HW 1 - due***
4 ***Feb. 5***	MOS Transistor Theory, MOS Device IV characteristics, MOS DC Characteristics.	Chapter 3
5 ***Feb. 12***	MOS Transistor Theory, Capacitance, Threshold voltage, Body effect, Channel Length Modulation, Scaling.	Chapter 3 ***HW 2 - due***
6 ***Feb. 19***	Capacitances, Inverter DC voltage Characteristics, Transmission Gates. Inverter Current characteristics	Chapter 5, Chapter 6
7 ***Feb. 26***	Continue Inverter DC voltage characteristics, Inverter operation regions.	Chapter 6 ***Lab 1 - due***
8 ***Mar. 4***	Inverter dynamic behavior, Inverter Fall Time, Inverter Rise time, Inverter Delay.	Chapter 6 ***HW 3 - due***
9 ***Mar. 11***	**Midterm Exam I Friday, March 11, 9:30-11:30 am**	**Chapters 2, 3, 5, 6**
10 ***Mar. 25***	Delay and Inverter Optimizations, Sequential circuits and Interconnect Delay	Chapter 6 ***HW 4 -due***
11 ***April 1***	Interconnect Resistance and capacitances, Interconnect modeling, delay due to Interconnect	Course Notes, Chapter 6
12 ***April 8***	Supper buffer Design, Ring Oscillators, chip inverter delay estimations, Power consumption.	Chapter 6 ***Lab 2 - due***
13 ***April 15***	Power Consumption, Dynamic Circuits, Domino Logic	Chapter 6 ***HW 5 – due***
14 ***April 22***	Domino logic, Memory circuits, Memory cell, and Advanced Topics.	Chapter 9
15 ***April 29***	Phase-Locked Loop opeartion, Clock Recovery, Digital Phase looked loop, VCO, Divider, Loop Filter.	Class Notes ***HW 6 – due***
Final Exam Week	**Midterm Exam II (Final Exam) Friday, ???? , 9:30 – 11:30 am** ========== **Final Project - due the last day of school Date and time: To be announced**	**Chapters 6 and 9**