EE599 – Verification of VLSI Systems

Nazarian Summer 15

University of Southern California
Department of Electrical Engineering

Course Description

This is a 4-unit course on the verification tools and concepts used to detect design errors or bugs of VLSI circuits and systems that may impact functionality, timing, and power. Tasks required for the labs and projects include design and verification using SystemC or SystemVerilog, simulation-based, semi-formal and formal verification tools, and standard methodologies, such as OVM/UVM, etc.

Website

https://blackboard.usc.edu/

Course Material

- Lecture slides (which will be posted on course page) and class notes.
- Supplemental material (research papers, technical articles, etc.) will be provided.

Prerequisite

There is no prerequisite for this course, however strong programming skills is highly recommended.
D-clearance will be issued in late April or early May. The minimum requirement is an A in EE577A or CS570 or 577B or 557 and also passing an interview which will be scheduled for late April or early May.

Topics and Schedule

Will be presented in detail during interview and also posted when finalized in early May.

Instructor

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