UNIVERSITY OF SOUTHERN CALIFORNIA
USC VITERBI SCHOOL OF ENGINEERING
MING HSIEH DEPARTMENT OF ELECTRICAL ENGINEERING

EE 348: #30708R **FALL, 2013**
COURSE SYLLABUS **J. CHOMA**

ABSTRACT:

EE 348 establishes a foundation for integrated electronic circuit design. The course examines the fundamental circuit cells that underpin the realization of analog electronic circuits and systems. Most of the circuits addressed exploit metal-oxide-semiconductor field-effect transistor (MOSFET) devices, but some attention is also given to bipolar junction transistor (BJT) technology. The fundamental tools exploited to study these electronic devices, networks, and systems derive largely from the theoretic concepts and analytical strategies developed in the first circuits course, which is EE 202 at USC.

Design is a challenging undertaking because it is not the straightforward problem of finding the N solutions to a system of N equations in N unknowns. The most typical design problem is one in which there are more specifications that must be satisfied and/or more variables that need to be determined than there are independent equations that can be written. Basic algebra teaches that a problem for which the number of unknowns does not equal the number of available independent equations has no unique solution. It follows that a single, and therefore unique, design solution is rare. Among the set of non-unique solutions that are viable in the sense that they satisfy most, if not all, of the target specifications of a circuit, some are arguably better than others. For example, some solutions dissipate lower power than do others, some boast input/output (I/O) operating properties that are less sensitive to manufacturing uncertainties than are others, and some generate less electrical noise and/or response distortion than do others. The best of these design solutions are not forged by trial and error strategies. Instead, optimal designs derive from the fruits of fundamentally understanding relevant circuit and system concepts. The task necessarily preceding an understanding of electronic engineering complexities is the conduct of thorough mathematical analyses and computer-based investigations that insightfully highlight both the attributes and the limitations of the circuits and systems under consideration. The satisfying understanding that underpins the execution of the genuinely difficult task of creative circuit design ensues when analytical disclosures can be lucidly interpreted and explained in terms of fundamental physical laws, basic circuit and system concepts, and minimal mathematical manipulations.

Because understanding is such a crucial ingredient of the design recipe, computational precision is rarely the core objective of design-oriented engineering circuit analysis. Instead, analyses are conducted to gain insights into the circuit responses defined by the mathematical solutions for the electrical variables of a circuit. Insights are cultivated by conceptually comprehending solutions cast in forms that underscore circuit advantages, disadvantages, best case operating features, and worst-case response properties. In short, design skills are not necessarily nurtured by elegant mathematical disclosures of circuit responses. They are more likely to derive from approximate circuit solutions that, when correctly interpreted in light of meaningfully invoked approximations and an awareness of desired circuit and system operating constraints and specifications, paint an understandable engineering picture of circuit dynamics. EE 348 attempts to paint these images brightly.

1. COURSE OBJECTIVES

The objectives of *Electronic Circuits I (EE 348)* are as follows.

1.1. Forge an insightful understanding of the theories and concepts projected by both active and pas-

sive electrical networks. Included among these theories and concepts are Thévenin's theorem, Norton's theorem, superposition theory, the magnitude, phase, and group delay responses implicit to network transfer functions, the poles and zeros that mathematically define the frequency domain behavior of circuits, and the interrelationships between the steady state frequency and time domain responses of circuits. This understanding arguably comprises the analytical foundation that supports circuit design creativity and the innovative realization of reliable, reproducible, and efficiently operating networks.

1.2. Establish an understanding and appreciation of the basic physical properties and electrical characteristics of PN junction diodes, metal-oxide-semiconductor field-effect transistors (MOSFETs), and bipolar junction transistors (BJTs). Of particular interest are the relationships of key physical properties to observable circuit performance.

1.3. Develop mathematical modeling strategies for diodes and transistors. These models serve the engineering design process by establishing understandable electrical equivalent circuits that emulate, albeit approximately, the electrical properties of active devices and entire electronic systems.

1.4. Define, develop, and assess the fundamental circuit cells that underlie the implementation of analog electronic networks and systems realized in either MOSFET or BJT device technologies. The attention given to these basic circuit cells embraces a consideration of biasing strategies that reduce the impact of the nonlinearities that pervade all active devices. A consideration of these cells also includes a delineation of performance advantages and shortfalls that impact the observable operating features of the electronic signal processing networks in which such cells are embedded.

1.5. Provide a cursory exposure to the more advanced analog signal processing concepts that comprise the foci of succeeding electrical engineering coursework and indeed, the continually evolving electronics state of the art. These concepts include radio frequency (RF) amplifiers, broadband electronic networks, mixed signal (combined digital and analog signal processing on a single board or single chip) circuits, and adaptive electronic networks that compensate automatically for the vagaries of device processing, circuit processing and manufacturing, and the environment (temperature, electromagnetic interference, etc.).

2. COURSE ADMINISTRATION

The prerequisite for ***EE 348*** is EE 202. EE 338 is a recommended co-requisite. Course lectures are given on **Mondays and Wednesdays from 2:00 -to- 3:20 in Olin Hall of Engineering (OHE), Room #230**.

EE 348 **lectures commence on Monday, 26 August 2013, and end on Wednesday, 04 December 2013**. Students who are absent from a given lecture should arrange to retrieve any graded homework that may have been returned in class, as well as any notes, homework assignments, homework solutions, or other information that may have been posted on the web during their absence. All supplemental course notes, lecture aids (Acrobat PDF versions of PowerPoint presentations used in formal class lectures) homework assignments, homework solutions, and other information and material can be found at the private website, **www.jcatsc.com**.

The last day to drop the course without a *"W"* grade and receive a *100*% refund of assessed course fees is Friday, 13 September 2013. The last day to drop the class with a *"W"* grade is Friday, 15 November 2013. An **Incomplete *"IN"* course grade** is rarely given. An ***"IN"*** grade can be justified only in such substantiated exceptional cases as an extended student illness, a temporary physical disability, or a personal hardship experienced after the twelfth week of the semester (after 15 November 2013).

The final examination is scheduled for Monday, 16 December 2013, from 2:00 -to-

4:00 PM. The date and time of the final examination is established by University Administration and cannot be changed by the course instructor. A midterm examination is also planned. The tentative date of the midterm examinations, are announced well in advance of their administration. Optional review sessions in advance of formal examinations and/or other special sessions, which are designed to facilitate comprehension of especially difficult or esoteric technical material, may be scheduled aperiodically. Such scheduling is determined by the extent of student interest in such sessions, and they depend on the availability of a suitable campus classroom.

The results of the midterm examinations, the lab grade, and the final examination combine with averaged homework grades in accordance with the algorithm given below to determine the final course average for each student. It should be noted that a conscientious effort is made to have homework assignments complement lecture material and imminent examinations. Homework is assigned periodically, and solutions are generally posted at **www.jcatsc.com** within twenty-four *(24)* hours following the day on which assignments are handed in for grading.

MIDTERM EXAMINATION #1 GRADE:	***15%***
MIDTERM EXAMINATION #2 GRADE:	***20%***
FINAL EXAMINATION GRADE:	***30%***
LABORATORY GRADE:	***25%***
HOMEWORK GRADE:	***10%***

Examinations can never be made up, nor can they be administered in advance of the scheduled examination dates unless suitable arrangements are made with the course instructor. If a student fails to take either of the two midterm exams, his or her grade will be based on only two *(2)* examinations and on a normalized maximum score of either *85 or 80* (depending on which exam was missed), as opposed to *100*. **An automatic failure results if the student has a non-excused absence from both midterm examinations, and/or an absence from the final examination. An automatic failure also results if the laboratory component of the course is failed.** Kindly be aware that **Laboratory failure is assured** if any one of the laboratory assignments is not completed.

Prof. John Choma is the Course Instructor. The Teaching Assistant, whose responsibilities include teaching the laboratory component of the course and leading the weekly discussion session and grading homework assignments, will be identified shortly after the start of the semester. For the record, only the Course Instructor grades the midterm and final exams.

Faculty office hours are difficult to predict accurately, but nominal times for these hours **10:00 AM -to- 12:00 Noon on Tuesdays and 4:00 -to- 6:00 PM on Wednesdays**. Appointments for other meeting times can be arranged by e-mailing Prof. Choma at **johnc@usc.edu**. The Teaching Assistant will also post and maintain regular office hours.

3. Discussion Sections

Weekly discussion sections led by the Teaching Assistant are scheduled for **Mondays from 5:00 -to- 5:50 PM in Kaprielian Hall (KAP), Room #148**. Additional and optional discussion sections may be established as the semester progresses. Homework assignments are addressed in discussions, as is particularly challenging lecture material. During the first week of the fall 2013 semester, no discussion sections meet. Because the first week of class is a hectic period of time, no office hours are scheduled during the first full week of class.

4. LABORATORY SECTIONS

Each student is required to attend the laboratory section, which is scheduled as follows.

2:00 -to- 4:40 PM	***Friday***	***OHE #230***

The laboratory assignments are as itemized below.

[Experiment #0]. Overview Of Lab and *Introduction to SPICE*
[Experiment #1]. *Introduction to SPICE*
[Experiment #2]. *SPICE Simulations*
[Experiment #3]. *Op-Amp Theory and Applications*
[Experiment #4]. *Diodes*
[Experiment #5]. *MOSFETs: Static Operation*
[Experiment #6, 7] *MOSFETs*
[Experiment #8, 9]. *Introduction to Bipolar Junction Transistor (BJT) Amplifiers*

The specific objectives of all laboratory assignments will be addressed by the laboratory instructor in the actual laboratory sessions. Laboratory assignments focus on the development of circuit test methodologies, circuit analysis and assessment strategies, and circuit design skills. Collectively, they imbue students with a meaningful sampling of practical engineering design and characterization problems. Design projects, each entailing detailed analysis, engineering interpretation of analytical results, SPICE computer-aided circuit simulations, circuit construction, circuit test, and project reporting, are assigned as group undertakings.

Each student is required to purchase a proto board by the first laboratory meeting, which occurs during the week of 02 September 2013. Proto boards can be purchased in Olin Hall of Engineering (OHE) Room #246.

******An Absolute Prerequisite to Passing EE 348 Is That ALL Laboratory Assignments Must Be Completed!******

5. Study Guidelines and Suggestions

5.1. Spend time reading the *Abstract* of this Course Syllabus, which defines the pedagogy of *EE 348*. Conscientious students should understand that solutions to engineering analysis and design problems are not the dominant study issue. Particularly important is the ability to enable insightful interpretations of these solutions so that the fruits of analyses can foster innovative and creative circuit and system design. A matter related to interpretive acuity is the development of capabilities for defining, applying, and assessing meaningful analytical approximations, which are all but mandated if mathematical tractability and engineering understandability are to be achieved.

5.2. It is imprudent to view the *10%* weight attached to homework as being sufficiently small to warrant a tacit indifference to these assignments. When diligently addressed and considered, the assigned problems provide analytical experience and engineering insights that are foundational to a satisfying completion of the formal examinations. It should also be understood that homework is counted in the compilation of the final course grade only when its average score embellishes the final course average. When the homework average degrades an individual final course average, the homework score is not factored into the overall course average. In this case, the overall student average is based on an achievable maximum score of *90%*, as opposed to *100%*. In short, homework scores can only help the student's final grade.

5.3. Engineers rarely work independently. Accordingly, students are encouraged to work responsibly in both class homework assignments and lab work in teams that are no larger than four. It is assumed, of course, that such collaboration is done intelligently, conscientiously, and in a manner that encourages equal and proactive participation among all group members. Home-

work and lab teams need only hand in one assignment per group, making sure that the first page of each submitted assignment clearly identifies the names and corresponding student identification numbers of all group participants. Each member of a given group receives the same numerical mark for the submitted assignment. Homework assignments are graded by the Discussion Leader. On the other hand, examinations are graded exclusively by Prof. Choma.

5.4. Do not fall behind in the course lectures and assignments! Upper division electrical engineering classes, such as *EE 348*, are hierarchical; that is, the ability to understand material presented in any given week relies strongly on the comprehension of relevant technical matter discussed in preceding lectures or addressed in earlier homework assignments.

5.5. Try not to miss any scheduled classes, any discussion classes, or any supplementary discussion sections that may be offered! Lectures in courses like *EE 348* tend to inspire conversations about important tangential material that may not be explicitly addressed in the assigned readings.

5.6. Do not be shy in the classroom about asking questions about material that you do not comprehended. If you are unable to understand something well, chances are that others in class are experiencing similar confusion. Do not be shy about asking for additional assistance and visiting John Choma during regular office hours or at times arranged otherwise by appointment.

6. Required Readings and Suggested References

There is no formally assigned textbook for the class. But "Lecture Supplements," predicated largely on a forthcoming undergraduate text authored by Choma, are provided. References to these "Lecture Supplements" are prefaced with "*LS #X*" in the *Course Schedule*. "Lecture Aids" are abbreviated lecture supplements in PowerPoint form and are essentially notes and guidelines that support particular classroom lectures and discussions. These are indicated as ***"LA #X"*** in the Course Schedule. These supplements *(LS #X)* and aids ***(LA #X)***, whose titles are itemized below are available online at **www.jcatsc.com**. Other notes or relevant additional technical information may be added to the subject website as the fall 2013 semester progresses.

6.1. Lecture Aids *[Many of these "Aids" will be revised and updated during the Fall 2013 semester.]*

[LA #1]. *Review of Fundamental Circuit Theory and Concepts*
[LA #2]. *PN Junction Diode Models and Circuit Applications*
[LA #3]. *Circuit Level Models of MOS Technology Transistors*
[LA #4]. *MOSFET Technology Biasing Networks*
[LA #5]. *Canonic Analog MOSFET Circuit Cells at Low Frequencies*
[LA #6]. *Models and Characteristics of Integrated Bipolar Transistors*
[LA #7]. *Biasing Circuits for Bipolar Junction Transistors*
[LA #8]. *Canonic Analog BJT Circuit Cells At Low Frequencies*
[LA #9]. *Broadband Integrated Bipolar Transistor Circuits*

6.2. Lecture Supplements *[Some of these "Supplements" may be updated during the Fall 2013 semester.]*

[LS #1]. *Circuit and System Fundamentals* (co-authored with W-K. Chen)
[LS #2]. *Two-Port and Basic Amplifier Networks*
[LS #3]. *PN Junction Diodes*
[LS #4]. *Circuit Level Models and Basic Applications of MOS Technology Transistors*
[LS #5]. *Bipolar Junction Transistor Models and Biasing Circuits*
[LS #6]. *Canonic Cells of Analog MOS/CMOS Technology*
[LS #7]. *Canonic Circuit Cells of Analog BJT Technology*

6.3. Recommended Reference Textbooks

P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. New York: Oxford University Press, 2002.

M. Burns and G. Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*. New York: Oxford University Press, 2001.

W-K. Chen, L. O. Chua, J. Choma, Jr., and L. P. Huelsman (editors), *The Circuits and Filters Handbook*. Boca Raton, Florida: CRC/IEEE Press, 1995.

J. Choma, Jr., *Electrical Networks*. New York: Wiley–Interscience, 1985.

J. Choma and W-K. Chen, *Feedback Networks: Theory and Circuit Applications*. Singapore: World Scientific Press, 2007

K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*. Reading, Massachusetts: Addison-Wesley Pub. Co., 1978.

D. Clein, *CMOS IC Layout: Concepts, Methodologies, and Tools*. Boston: Butterworth-Heinemann (Newnes), 2000.

D. T. Comer, *Introduction to Mixed Signal VLSI*. Highspire, Pennsylvania: Array Publishing Co., 1994.

J. A. Connelly and P. Choi, Macromodeling with SPICE. Englewood Cliffs, New Jersey: Prentice-Hall, Inc., 1992.

R. C. Dorf (editor), *The Electrical Engineering Handbook*. Boca Raton, Florida: CRC Press, 1993.

D. P. Foty, *MOSFET Modeling With SPICE: Principles and Practice*. Upper Saddle River, New Jersey: Prentice Hall PTR, 1997.

R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI Design Techniques For Analog And Digital Circuits*. New York: McGraw-Hill Publishing Company, 1990.

P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer. *Analysis and Design of Analog Integrated Circuits* (4th Edition). New York: John Wiley & Sons, Inc.

A. B. Grebene, *Bipolar and MOS Analog and Integrated Circuit Design*. New York: Wiley–Interscience, 1984.

R. Gregorian and G. C. Temes, *Analog MOS Integrated Circuits for Signal Processing*. New York: Wiley–Interscience, 1986.

R. J. Higgins, *Electronics With Digital and Analog Electronics*. Englewood Cliffs, New Jersey: Prentice Hall, Inc., 1983.

R. T. Howe and C. G. Sodini, *Microelectronics: An Integrated Approach*. Upper Saddle River, New Jersey: Prentice Hall, Inc., 1997.

J. H. Huijsing, R. J. van der Plassche, and W. Sansen (editors), *Analog Circuit Design*. Boston: Kluwer Academic Publishers, 1993.

R. C. Jaeger, *Microelectronic Circuit Design*. New York: McGraw-Hill, 1997.

D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: John Wiley and Sons, Inc., 1997.

K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems*. New York: McGraw-Hill, Inc., 1994.

T. H. Lee, *The Design Of CMOS Radio–Frequency Integrated Circuits*. Cambridge, United Kingdom: Cambridge University Press, 2004.

W. Liu, *MOSFET Models for SPICE Simulation*. New York: John Wiley and Sons, Inc., 2001.

G. Palumbo and A. Pennisi, *Feedback Amplifiers: Theory and Design*. Boston: Kluwer Academic Publishers, 2002.

D. O. Pederson and K. Mayaram, *Analog Integrated Circuits for Communication*. Boston: Kluwer Academic Publishers, 1991.

E. Sánchez-Sinencio and A. G. Andreou (editors), *Low-Voltage/Low-Power Integrated Circuits and Systems*. New York: IEEE Press, 1999.

T. F. Schubert, Jr. and E. M. Kim, *Active and Non–Linear Electronics*. New York: John Wiley & Sons, Inc., 1996.

M. H. Rashid, *Microelectronic Circuits: Analysis and Design*. Boston: PWS Publishing Company, 1999.

B. Razavi, *Fundamentals of Microelectronics (2nd Edition)*. New York: John Wiley & Sons, Inc., 2014.

7. Course Schedule

WEEK	WEEK OF	LECTURE TOPIC	READINGS
1, 2	08/26/2013 09/02/2013	**CIRCUIT ANALYSIS REVIEW** Thévenin's and Norton Theorems Basic Electronic System Concepts Steady State Sinusoidal Analysis Model Relationship to Device Geometries Transient Analysis *Rise and Fall Times* *Settling Time* *Underdamped Step Response* *Overdamped Step Response* *Critically Damped Step Response*	**LS #1** **LS #2** **LA #1**
3	09/09/2013	**ANALOG SIGNAL PROCESSING** Voltage and Current Amplifiers Transadmittance (Transconductance) Amplifier Transimpedance (Transresistance) Amplifier Simple Filter	**LS #1** **LS #2** **LA #1**
4	09/16/2013	**RECTIFIERS AND SIMPLE POWER SUPPLIES** Half Wave Rectifier Full Wave Rectifier Lowpass RC And RL Filters Rectifier Transient Step Response	**LS #3** **LA #2**
5, 6, 7	09/23/2013 09/30/2013 10/07/2013	**MOS DEVICE MODELS AND BIASING** Long Channel Approximation (Shichman-Hodges) Models For Submicron Channels Small Signal Model High Frequency Performance Metrics Biasing For Nominally Linear Operation *Constant Current Sources And Sinks* *Supply Independent Biasing*	**LS #4** **LA #3** **LA #4**
6	**10/02/2013**	***MIDTERM EXAMINATION #1 Open Notes & Book***	
7, 8, 9, 10	10/07/2013 10/14/2013 10/21/2013 10/28/2013	**CANONIC CELLS OF ANALOG MOS** Common Source Amplifier Common Drain Amplifier Common Gate Amplifier Conventional and Regulated Cascodes Balanced Differential Amplifier	**LS #6** **LA #5** **LA #4**
11, 12	11/04/2013 11/11/2013	**BIPOLAR MODELS AND BIASING** Qualitative Description of Physical Operation Ebers-Moll Model Gummel-Poon Model Biasing Small signal Model *Global and Local Feedback* *Dual Loop Feedback* Circuit Examples	**LS #5** **LA #6** **LA #7**
11	**11/06/2013**	***MIDTERM EXAMINATION #2 Open Notes & Book***	

WEEK	WEEK OF	LECTURE TOPIC	READINGS
13, 14, 15	11/18/2013 11/252013 12/02/2013	**CANONIC CELLS OF ANALOG BIPOLAR** Common Emitter Amplifier Common Collector Amplifier Common Base Amplifier Cascode Configurations Balanced Differential Amplifier	**LS #7** **LA #7** **LA #8** **LA #9**
	12/16/2013 **Last Regular Class**, ***12/04/2013***	***FINAL EXAMINATION*** ***(2:00 -to- 4:00 PM)***	***Open Notes,*** ***Open Book***

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05 August 2013

cc. **Prof. E-S. Kim**, Department Chair
Prof. E. Maby, Associate Department Chair
EE 348–Website