EE 677: VLSI ARCHITECTURES AND ALGORITHMS

Prof. Viktor Prasanna
MW 330-450, FALL 2012

Reconfigurable computing based on Field Programmable Gate Arrays (FPGAs) is attractive for implementing many application-specific solutions including embedded computing applications. The focus of the course will be **reconfigurable computing systems** addressing devices, systems, and application synthesis and analysis. The course will cover the following topics:

1. **Introduction to Reconfigurable Computing:** Motivation, architectures, static and dynamic reconfiguration, reconfiguration costs and models, building blocks of programmable logic devices. Computational models of reconfigurable computing systems.
2. **Field Programmable Gate Arrays (FPGAs):** State-of-the-art devices, device characteristics, fine grain and coarse grain devices, illustrative features of Xilinx Virtex and Altera Stratix family of devices.
3. **Design Flow for Application Synthesis:** Compilation/synthesis tools, system level design tools, domain specific tools, and illustrative examples.
4. **Architectures and Algorithms for Computing Kernels:** Tradeoffs in implementing various kernels: matrix multiplication, pattern matching, FFT, reduction, etc. Implementation and performance analysis.
5. **Embedded Computing using Reconfigurable Devices:** Application directed architectures, soft processors, energy optimization, performance models and benchmarks, illustrative examples from adaptive signal processing, software defined radio, intrusion detection, high speed networking. Performance comparison with DSPs and embedded processors.
6. **High end Computing using Reconfigurable Devices:** Architecture of FPGA augmented high end systems, parameterized IP, floating point cores, energy, latency and throughput optimizations, tradeoffs in synthesizing scientific kernels.
7. **Current topics in using Reconfigurable Hardware:** Programming models, IP cores, FPGA inspired computing models, energy efficiency, high level tools.

TEXT: We will borrow from recent literature. Reading list will be handed out in the class.

REFERENCE: Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays by Maya Gokhale and Paul S. Graham, *Springer*, 2005.

ACTIVITIES: In addition to participation in-class discussions, students are expected to read and summarize several articles, use FPGA based boards and software tools in our lab, explore novel applications of these devices, and also use possible remote access to supercomputers based on FPGAs. In addition to lectures by the instructor there will be guest lectures by leading researchers from industry and national labs.

COURSE GRADE: Based on homework assignments (approx. 5), implementation projects (approx. 4), mid term, term project and presentation.

PREREQUISITE: This course will involve analysis of various tradeoffs as well as actual implementations using design tools. EE 557 and CS 570 are required background courses. Check with the instructor if you have not taken any of these courses. EE577a/b are NOT required prerequisites.

Please direct any inquiries concerning this course to Prof. Viktor Prasanna, prasanna@usc.edu, x04483, EEB-200C.