UNIVERSITY OF SOUTHERN CALIFORNIA
USC VITERBI SCHOOL OF ENGINEERING
MING HSIEH DEPARTMENT OF ELECTRICAL ENGINEERING

EE 348: #30474R **SPRING, 2012**
COURSE SYLLABUS **CHOMA**

ABSTRACT:

EE 348 establishes a foundation for integrated electronic circuit design. The course examines the fundamental circuit cells that underpin the realization of analog electronic circuits and systems. Many of the circuits addressed exploit metal-oxide-semiconductor field-effect transistor (MOSFET) devices, but attention is also given to bipolar junction transistor (BJT) technology. The fundamental tools exploited to study these electronic devices, networks, and systems derive largely from the theoretic concepts and analytical strategies developed in the first circuits course, which is EE 202 at USC.

Design is a challenging undertaking because it is not the straightforward problem of finding the N solutions to a system of N equations in N unknowns. The most typical design problem is one in which there are more specifications that must be satisfied and/or more variables that need to be determined than there are independent equations that can be written. Basic algebra teaches that a problem for which the number of unknowns does not equal the number of available independent equations has no unique solution. It follows that a single, and therefore unique, design solution is rare. Among the set of non-unique solutions that are viable in the sense that they satisfy most, if not all, of the target specifications of a circuit, some solutions are arguably better or more desirable than others. For example, some solutions dissipate lower power than do others, some boast input/output (I/O) operating properties that are less sensitive to manufacturing uncertainties than are others, and some generate less electrical noise or response distortion than do others. The best of these design solutions are not forged by trial and error strategies. Instead, optimal designs derive from the fruits of fundamentally understanding relevant circuit and system concepts. The task necessarily preceding an understanding of electronic engineering complexities is the conduct of thorough mathematical and computer-based analyses that insightfully highlight both the attributes and the limitations of the circuits and systems under consideration. The satisfying understanding that underpins the execution of the genuinely difficult task of creative circuit design ensues when analytical disclosures can be creatively interpreted and lucidly explained in terms of fundamental physical laws, basic circuit and system concepts, and minimal mathematics.

Because understanding is such a crucial ingredient of the design recipe, computational precision is rarely the core objective of design-oriented engineering circuit analysis. Instead, analyses are conducted to gain insights into the circuit responses defined by the mathematical solutions for the electrical variables of a circuit. Insights are cultivated by conceptually comprehending solutions cast in forms that underscore circuit advantages, disadvantages, best case operating features, and worst-case response properties. In short, design skills are not necessarily nurtured by elegant mathematical disclosures of circuit responses. They are more likely to derive from approximate circuit solutions that, when correctly interpreted in light of meaningfully invoked approximations and an awareness of desired circuit and system operating constraints and specifications, paint an understandable engineering picture of circuit dynamics. EE 348 paints these images.

1. COURSE OBJECTIVES

The fundamental objectives of *Electronic Circuits I (EE 348)* are as follows.

1.1. Forge an insightful understanding of the theories and concepts projected by both active and passive electrical networks. Included among these theories and concepts are Thévenin's theorem, Norton's theorem, superposition theory, the magnitude and phase responses implicit to network transfer functions, the poles and zeros that mathematically define the frequency domain behavior of circuit structures, and the interrelationships between the steady state frequency and time domain responses of circuits. This understanding arguably comprises the analytical foundation that supports circuit design creativity and the innovative realization of reliable, reproducible, and efficiently operating networks.

1.2. Establish an understanding and appreciation of the basic physical properties and electrical characteristics of PN junction diodes, metal-oxide-semiconductor field-effect transistors (MOSFETs), and bipolar junction transistors (BJTs).

1.3. Develop mathematical modeling strategies for diodes and transistors. These models serve the engineering design process by establishing understandable electrical equivalent circuits that emulate, albeit approximately, the electrical properties of active devices and entire electronic systems.

1.4. Define, develop, and assess the fundamental circuit cells that underlie the implementation of analog electronic networks and systems realized in either MOSFET or BJT device technologies. The attention given to these basic, or canonic, circuit cells embraces a consideration of biasing strategies that reduce the impact of the nonlinearities pervasive of all active devices. A consideration of these cells also includes a delineation of performance advantages and shortfalls that impact the observable operating features of the electronic signal processing networks in which such cells are embedded.

1.5. Provide a cursory exposure to the more advanced analog signal processing concepts that comprise the foci of succeeding electrical engineering coursework and indeed, the continually evolving electronics state of the art. These concepts include radio frequency (RF) amplifiers, broadband electronic networks, mixed signal (combined digital and analog signal processing on a single board or single chip) circuits, and adaptive electronic networks that compensate automatically for the vagaries of device processing, circuit processing and manufacturing, and the environment (temperature, electromagnetic and electrical interference, etc.).

2. COURSE ADMINISTRATION

The prerequisite for EE 348 is EE 202. EE 338 is a desirable co-requisite. Course lectures are given on **Tuesdays and Thursdays from 11:00 -to- 12:20 in Kaprielian Hall (KAP), Room #147**.

EE 348 lectures commence on Tuesday, 10 January 2012 and end on Thursday, 26 April 2012. Students who are absent from particular lecture or discussion sessions should arrange for a friend to provide any notes, homework assignments, homework solutions, or other information distributed during their absence. A website for EE 348 (www.jcatsc.com) is available to students for convenient access to lecture notes, homework assignments and solutions, and laboratory assignments.

The last day to drop the course without a *"W"* grade and receive a 100% refund of assessed course charges is Friday, 27 January 2012. The last day to drop the class with a *"W"* grade is Friday, 06 April 2012. An **Incomplete *"IN"*** course grade is rarely given. An ***"IN"*** grade can be justified only in substantiated exceptional cases such as an extended student illness, a temporary physical disability, or a personal hardship experienced after the twelfth week of the semester (after 06 April 2012).

The final examination is scheduled for Tuesday, 08 May 2012, from 11:00 AM -to- 1:00 PM. Two midterm examinations are also scheduled. After hours optional review sessions for impending examinations may be scheduled two to three lecture days before the date of an

exam. Other optional review sessions can be given, pending student interest, student need, and instructor availability.

Homework is assigned nominally weekly, and solutions are normally posted on the course web site (www.jcatsc.com) by the day following the day on which assignments are handed in. Conscientious efforts are made to have homework assignments complement the lecture material and assigned laboratory work. These homework assignments are compiled to provide students with meaningful analytical (both manual and computer-aided) experiences that help to prepare them for examinations. **Completed homework assignments are never accepted after the due date**. To compensate for this inflexibility, the final homework average is factored into the compilation of the final course average only if the homework grade enhances the overall course average.

The results of the two *(2)* midterm examinations, the final examination, and averaged homework grades combine with the laboratory grade in accordance with the algorithm given below to determine the final course average for each student.

MIDTERM EXAMINATION #1 GRADE:	***15%***
MIDTERM EXAMINATION #2 GRADE:	***20%***
FINAL EXAMINATION GRADE:	***30%***
LABORATORY GRADE:	***20%***
HOMEWORK GRADE:	***15%***

Examinations can never be made up, nor can they be administered in advance of the scheduled examination date unless suitable arrangements are made with the course instructor. **The date and time of the final examination is established by University Administration and cannot be altered.** If a student fails to take either of the two midterm exams, his or her grade will be based on only two *(2)* examinations and on a normalized maximum score of either *85 or 80* (depending on which exam was missed), as opposed to *100*. **An automatic failure results if the student has a non-excused absence from both midterm examinations, and/or an absence from the final examination. An automatic failure also results if the laboratory component of the course is failed.** Kindly note that **Laboratory failure is ensured** if any one of the laboratory assignments is not completed.

Prof. John Choma is the course instructor, and **Mr. Aaron Curry** is the Discussion Section Leader and Laboratory Instructor. Aaron, who has taken several graduate and undergraduate courses from Dr. Choma, is familiar with what Dr. Choma expects of his students. He has been encouraged to share this familiarity with all EE 348 students.

Prof. Choma's office hours are difficult to predict accurately but generally, they are from 12:00 -to- 2:00 on Mondays and from 1:00 -to- 3:00 on Tuesdays in Powell Hall of Engineering **(PHE) Room #620**. Appointments for other meeting times can be arranged by telephoning Prof. Choma at **213-740-4692** or by e-mailing him at **johnc@usc.edu**. Aaron Curry will also establish regular office hours.

3. DISCUSSION SECTIONS

Each student is required to attend the weekly discussion section, which is offered as follows.

5:00 -to- 5:50	***Monday***	***KAP***	***#147***

Homework and laboratory assignments are addressed in the discussion sections, as is particularly challenging lecture material. Discussion and laboratory sections begin meeting during the second week of the semester (week of 16 January 2012).

4. LABORATORY SECTIONS

Each student is required to attend the laboratory section, which is scheduled as follows.

6:00 PM -to- 8:40 PM	***Tuesday***	***OHE***	***#230***

The general nature and specific objectives of all laboratory assignments will be addressed by Aaron Curry in the actual laboratory sessions. These assignments focus on the development of circuit test methodologies, circuit analysis and assessment strategies, and circuit design skills. Collectively, they imbue students with a meaningful sampling of practical engineering design and characterization problems. Several design projects, each entailing detailed analysis, engineering interpretation of analytical results, SPICE computer-aided circuit simulation, circuit construction, circuit test, and project reporting, are assigned as group undertakings.

Each student is required to purchase a proto board by the first laboratory meeting, which occurs during the week of 16 January 2012. Proto boards can be purchased in Olin Hall of Engineering (OHE) Room #246.

******An Absolute Prerequisite to Passing EE 348 Is That**
All Laboratory Assignments Must Be Completed!****

5. STUDY GUIDELINES AND SUGGESTIONS

5.1. Read the *Abstract* of this Course Syllabus, which defines the course instructor's pedagogy. Fundamentally, it conveys the notion that the solutions to problems are not the only important issue. Equally important is the ability to develop the engineering insights that forge creative and meaningful circuit and system design skills. A matter related to interpretive acuity is the development of expertise for defining, applying, and assessing meaningful analytical approximations, which you will discover are essential if mathematical tractability and engineering understandability are to be achieved.

5.2. It is imprudent and potentially disastrous to view the *15%* weight attached to homework as being sufficiently small to warrant its tacit neglect. Many of the problems assigned derive from EE 348 examinations administered in previous semesters, and most, when thoroughly addressed and considered, provide you with the analytical experience and engineering insights that are likely to foster self-confidence during examinations.

5.3. Engineers rarely work independently. Accordingly, students are encouraged to work in small teams (no larger than four) on homework assignments, assuming, of course, that such collaboration is done intelligently, conscientiously, and in a manner that encourages academic synergy among all group members. If you choose to work in homework teams, you need hand in only one assignment per group, making sure that the first page of each submitted assignment clearly identifies all group members and their respective student identification numbers. Each member of a given group receives the same numerical mark for the given submission.

5.4. Do not fall behind in the course lectures, the homework assignments, and the laboratory assignments! Upper division electrical engineering classes, such as EE 348, are hierarchical; that is, the ability to understand material presented in any given week relies strongly on your comprehension of technical matter discussed in preceding weeks.

5.5. Do not miss class! The instructor rarely follows the assigned reading material closely and has no reservations about compiling homework assignments and examinations predicated, at least in part, on material discussed in class but not addressed in said reading material.

5.6. Do not be shy in the classroom about asking questions about material you do not clearly comprehend. If you do not understand something, chances are that many of your peers share your miscomprehension. Do not be shy about coming to the Choma's office for additional assistance, and do not hesitate to ask Aaron Curry for help. As noted earlier, Aaron Curry has complete liberty to address course issues in any manner he deems appropriate. This discretionary latitude includes sharing with you any insights he may have garnered about Choma's grading, lecturing, and examination styles.

6. REQUIRED TEXT and SUGGESTED REFERENCES

There is no formally assigned textbook for the class. But "Lecture Supplements," predicated largely on a forthcoming Cambridge University text authored by Choma, are provided. References to these "Lecture Supplements" are prefaced with *"LS"* in the *Course Schedule*. "Lecture Aids" are abbreviated Lecture Supplements in PowerPoint form and are essentially notes and guidelines that support particular classroom lectures and discussions. These are indicated as *"LA"* in the Course Schedule. These supplements **(LS #)** and aids **(LA #)**, whose titles are itemized below are available online at **www.jcatsc.com**. Other notes or relevant other technical information are likely to be added to the subject website as the spring semester progresses.

[LS1] J. Choma and W-K Chen, *Circuit and System Fundamentals*, pp. 1-88
[LS2] J. Choma, *Two-Port and Basic Amplifier Networks*, pp. 89-171
[LS3] J. Choma, *PN Junction Diodes*, pp. 172-263
[LS4] J. Choma, *Circuit Level Models and Basic Applications of MOS Technology Transistors*, pp. 264-346
[LS5] J. Choma, *Bipolar Junction Transistor Models and Biasing Circuits*, pp. 347-451
[LS6] J. Choma, *Canonic Cells of Analog MOS/CMOS Technology*, pp. 452-546
[LS7] J. Choma, *Canonic Circuit Cells of Analog BJT Technology*, pp. 547-TBD

[LA1] J. Choma, *Review of Fundamental Circuit Theory and Concepts*, slides 1-41
[LA2] J. Choma, *PN Junction Diode Models and Circuit Applications*, slides 41-63
[LA3] J. Choma, *Circuit Level Models of MOS Technology Transistors*, slides 64-111
[LA4] J. Choma, *MOSFET Technology Biasing Networks*, slides 112-143
[LA5] J. Choma, *Canonic Analog MOSFET Circuit Cells at Low Frequencies*, slides 144-232
[LA6] J. Choma, *Models and Characteristics of Integrated Bipolar Transistors*, slides 233-279
[LA7] J. Choma, *Biasing Circuits for Bipolar Junction Transistors*, slides 280-327
[LA8] J. Choma, *Canonic Analog BJT Circuit Cells At Low Frequencies*, slides 328-417
[LA9] J. Choma, *Broadband Integrated Bipolar Transistor Circuits*, slides 418-466

The following textbooks contain potentially beneficial reference reading material.

Phillip E. Allen and Douglas R. Holberg, *CMOS Analog Circuit Design*. New York: Oxford University Press, 2002.

M. J. Buckingham, *Noise in Electronic Devices and Systems*. Chichester, United Kingdom: Ellis Horwood Limited Publishers, 1983.

Mark Burns and Gordon Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*. New York: Oxford University Press, 2001.

W-K Chen, L. O. Chua, J. Choma, Jr., and L. P. Huelsman (editors), *The Circuits And Filters Handbook*. Boca Raton, Florida: CRC/IEEE Press, 1995.

J. Choma, Jr., *Electrical Networks*. New York: Wiley–Interscience, 1985.

J. Choma and W-K. Chen, *Feedback Networks: Theory and Applications*. Singapore: World Scientific Press, 2007.

K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*. Reading, Massachusetts: Addison-Wesley Pub. Co., 1978.

Dan Clein, *CMOS IC Layout: Concepts, Methodologies, and Tools*. Boston: Butterworth-Heinemann (Newnes), 2000.

Donald T. Comer, *Introduction To Mixed Signal VLSI*. Highspire, Pennsylvania: Array Publishing Co., 1994.

J. A. Connelly and P. Choi, Macromodeling With SPICE. Englewood Cliffs, New Jersey: Prentice-Hall, Inc., 1992.

R. C. Dorf (editor), *The Electrical Engineering Handbook*. Boca Raton, Florida: CRC Press, 1993.

Daniel P. Foty, *MOSFET Modeling With SPICE: Principles and Practice*. Upper Saddle River, New Jersey: Prentice Hall PTR, 1997.

S. Franco, *Design With Operational Amplifiers and Analog Integrated Circuits*. New York: McGraw-Hill, 2002.

R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI Design Techniques For Analog And Digital Circuits*. New York: McGraw-Hill Publishing Company, 1990.

P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: John Wiley & Sons, Inc., 2001.

A. B. Grebene, *Bipolar and MOS Analog and Integrated Circuit Design*. New York: Wiley–Interscience, 1984.

Roubik Gregorian and Gabor C. Temes, *Analog MOS Integrated Circuits for Signal Processing*. New York: Wiley–Interscience, 1986.

Roger T. Howe and Charles G. Sodini, *Microelectronics: An Integrated Approach*. Upper Saddle River, New Jersey: Prentice Hall, Inc., 1997.

Johan H. Huijsing, Rudy J. van der Plassche, and Willy Sansen (editors), *Analog Circuit Design*. Boston: Kluwer Academic Publishers, 1993.

Mohammed Ismail and Terri Fiez (editors), *Analog VLSI Signal And Information Processing*. New York: McGraw-Hill, Inc., 1994.

Richard C. Jaeger, *Microelectronic Circuit Design*. New York: McGraw-Hill, 1997.

D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: John Wiley and Sons, Inc., 1997.

S-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*. New York: McGraw-Hill, 2003.

Kenneth R. Laker and Willy M. C. Sansen, *Design of Analog Integrated Circuits and Systems*. New York: McGraw-Hill, Inc., 1994.

B. P. Lathi, *Modern Digital and Analog Communication Systems*. New York: Oxford University Press, 1998.

William Liu, *MOSFET Models for SPICE Simulation*. New York: John Wiley and Sons, Inc., 2001.

Gaetano Palumbo and Salvatore Pennisi, *Feedback Amplifiers: Theory and Design*. Boston: Kluwer Academic Publishers, 2002.

Sunggu Lee, *Design of Computers and Other Complex Devices*. Upper Saddle River, New Jersey: Prentice-Hall, 2000.

Thomas H. Lee, *The Design Of CMOS Radio–Frequency Integrated Circuits*. Cambridge, United Kingdom: Cambridge University Press, 2004.

William Liu, *MOSFET Models for SPICE Simulation, Including BSIM3v3 and BSIM4*. New York: Wiley-Interscience, 2001.

B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.

Edgar Sánchez-Sinencio and Andreas G. Andreou (editors), *Low–Voltage/Low–Power Integrated Circuits and Systems*. New York: IEEE Press, 1999.

Thomas F. Schubert, Jr. and Ernest M. Kim, *Active and Non–Linear Electronics*. New York: John Wiley & Sons, Inc., 1996.

G. C. Temes and J. W. LaPatra, *Introduction to Circuit Synthesis and Design*. New York: McGraw-Hill Book Company, 1977.

7. EE 348 SPRING 2012 COURSE SCHEDULE

WEEK	WEEK OF	LECTURE TOPIC	READINGS
1, 2	01/09/12 01/16/12	**CIRCUIT ANALYSIS REVIEW** Thévenin's and Norton's Theorems Basic Electronic System Concepts Steady State Sinusoidal Analysis Transient Analysis	LS1 LS2 LA1
3	01/23/12	**ANALOG SIGNAL PROCESSING** Voltage and Current Amplifiers Transadmittance (Transconductance) Amplifier Transimpedance (Transresistance) Amplifier Simple Filters	LS1 LS2 LA1
4	01/30/12	**RECTIFIERS AND SIMPLE POWER SUPPLIES** Half Wave Rectifier Full Wave Rectifier Capacitive Filter Diode Transient Response	LS3 LA2
5, 6, 7	02/06/12 02/13/12 02/20/12	**MOS TECHNOLOGY DEVICE MODELS** Long Channel Approximation Short Channel Approximation Small Signal Model High Frequency Performance Metrics Biasing For Linear Operation *Constant Current Sources* *Supply Independent Biasing*	LS4 LA3 LA4
6	**02/13/12**	***MIDTERM EXAMINATION #1 (02/16/12)***	**Open Notes**
7, 8, 9	02/20/12 02/27/12 03/05/12	**CANONIC ANALOG MOS CIRCUIT CELLS** Common Base Amplifier Common Drain Amplifier Regulated Cascode Current Sources And Sinks Balanced Differential Amplifiers	LS6 LA5
10	**03/12/12**	******SPRING BREAK ******	***NO CLASS****
10, 11, 12	03/19/12 03/26/12 04/02/12	**BIPOLAR DEVICE MODELS** Qualitative Operating Description Ebers-Moll Model Gummel-Poon Model Biasing Small–Signal Model	LS5 LA6
11	**03/26/12**	***MIDTERM EXAMINATION #2 (03/29/12)***	**Open Notes**
13, 14, 15	04/09/12 04/16/12 04/23/12	**CANONIC BIPOLAR CIRCUIT CELLS** Common Emitter Amplifier Common Base Amplifier Common Collector Amplifier Differential Architectures	LS7 LA7 LA8 LA9
	Last Class, 04/26/12	***FINAL EXAMINATION (05/08/12–11:00 to 1:00)***	**Open Notes**

John Choma, Professor
Ming Hsieh Department of Electrical Engineering
18 December 2011

cc. Prof. E. S. Kim, Department Chair
Dr. E. Maby (Associate Department Chair)
Mr. Aaron Curry (Teaching Assistant)
EE 348–Website