UNIVERSITY OF SOUTHERN CALIFORNIA
USC VITERBI SCHOOL OF ENGINEERING
MING HSIEH DEPARTMENT OF ELECTRICAL ENGINEERING

EE 541: #30704R/#30705R **FALL, 2011**
COURSE SYLLABUS **CHOMA**

ABSTRACT:

EE 541 addresses the analysis, design, and implementation of high performance analog filters suitable for data processing, information transmission, analog broadband networks, and radio frequency (RF) communication systems realized in modern monolithic circuit technologies. Several reasons underlie the necessity of suitable filters in these systems. Foremost among these reasons is that they can be used to modify circuit impedances to ensure the reasonably efficient transfer of signal power between driver and load ports or optimal noise performance. Maximum power transfer is a critical design objective in high frequency communication networks because the anemic levels of signal power indigenous to such systems increase the risk of contaminating signal information with omnipresent electrical noise. Filters can also be employed to improve the high frequency responses of active circuits by mitigating the deleterious impact of active device capacitances. They can even improve the observable linearity of certain types of active systems by achieving a sharp attenuation of the high frequency harmonics incurred by inherent active device nonlinearities. The RC and RLC filters implicit to electronic power supplies comprise simple examples of filters designed to obviate undesirable harmonics of power line frequencies. Finally, filters can annihilate unwanted signals by offering designable frequency selectivity. For example, lowpass filters all but eliminate undesired signal or noise energy at very high frequencies, bandpass filters offer frequency selective signal processing, as well as a reduction of cumulative output noise energy, and stopband filters obviate the energy of specific frequencies lying within the frequency spectra of the signal information earmarked for processing.

Active filters comprised of resistors, capacitors, and either operational amplifiers (op-amps) or operational transconductor amplifiers (OTAs) are widely used in audio, video, and other types of relatively low frequency signal processors. But for systems operating in the high hundreds of megahertz to- the tens of gigahertz, active filters are inappropriate because of the inadequate gain-bandwidth product, phase response, delay characteristics, and linearity metrics afforded by op-amps and OTAs. As a result, passive filtering networks containing resistors, capacitors, inductors, and even transformers and quasi-distributed transmission lines are commonplace in RF and ultra high frequency mixed signal integrated circuits. Indeed, and in stark contrast to more traditional very large scale integrated (VLSI) digital circuits, these monolithic RF units display a relatively high ratio of passive -to- active components. These latter (passive) filters comprise the dominant focus of EE 541.

The fundamental theories that underpin the design and realization of passive filters were largely forged four -to- six decades ago by such technical luminaries as Cauer, W-K. Chen, Darlington, Foster, Huelsman, S. K. Mitra, and others. One course is not a sufficient forum to address all of these seminal contributions. But since an insightful understanding of relevant circuit theoretic concepts is essential to the meaningful and efficient design of passive filters for RF systems, EE 541 does address essential theoretic issues. Included among these issues are two port networks, scattering analyses, parametric sensitivities, and distributed network analyses. The latter analyses are pivotal for a satisfying understanding of very high frequency circuit dynamics. Additionally, they form the basis for the design of distributed passive and active networks offering exciting I/O transfer characteristics, impedance matching, delay, and high frequency compensation attributes. The design strategies entail-

ing impedance matching, broadband network compensation, frequency response selectivity, and other types of filters are addressed definitively in this class.

Students enrolled in EE 541 must be comfortable with the technical material traditionally espoused in undergraduate courses on basic circuit theory, transformed frequency and time domains, and basic analog electronics in both MOS and bipolar technologies. The computer tools alluded to in the lectures and required in several homework assignments, include SPICE (conventional HSPICE or SPICE versions embedded within CADENCE, TANNER, TOPSPICE, or other design suites), MATLAB, and EXCEL.

1. Course Administration

The prerequisite for EE 541 is a basic undergraduate course in electronic circuits, such as EE 348 at USC. Course lectures are given on campus on Tuesdays and Thursdays from 12:30 -to- 1:50 PM in Olin Hall of Engineering (OHE), Room #120.

EE 541 lectures commence on Tuesday, 23 August 2011, and end on Thursday, 01 December 2011. Students who are absent from a given lecture should arrange for a colleague to obtain any notes, homework assignments, homework solutions, or other information that may have been distributed in class or posted on the web during their absence. On the rare occasion when hard copies of technical information are disseminated to students, extras of such material are not retained by the instructor. All supplemental course notes, lecture aids (PDF versions of PowerPoint presentations used in formal class lectures), homework assignments, homework solutions, and other information can be found at the website, **www.jcatsc.com**.

The last day to drop the course <u>without</u> a *"W"* grade is Friday, 09 September 2011. The last day to drop the class <u>with</u> a *"W"* grade is Friday, 11 November 2011. An **Incomplete *"IN"*** course grade is rarely given. An ***"IN"*** grade can be justified only in <u>substantiated exceptional cases</u> such as an extended student illness, a temporary physical disability, or a personal hardship experienced after the twelfth week of the semester (after 11 November 2011).

The final examination is scheduled for Tuesday, 13 December 2011, from 11:00 AM -to- 1:00 PM. One midterm examination is also planned. A <u>tentative</u> date for the midterm examination, which is announced well in advance of its administration, is Thursday, 13 October 2011. Optional review sessions in advance of formal examinations and/or as required, which are designed to facilitate comprehension of especially difficult technical material, may be scheduled aperiodically, pending the extent of student interest in such sessions and the availability of an appropriate Distance Education Network (DEN) classroom.

The results of the midterm examination and the final examination combine with averaged homework grades in accordance with the algorithm given below to determine the final course average for each student. It should be noted that a conscientious effort is made to have homework assignments complement lecture material and impending examinations. Homework is assigned periodically, and solutions are normally posted at **www.jcatsc.com** by the day following the day on which assignments are handed in for grading.

Examinations can never be made up, and homework solutions cannot be accepted late. If a student fails to take the midterm examination, his or her grade is based on a normalized maximum possible score of *75*, as opposed to the traditional maximum of *100*. **An auto-**

matic failure results if the student has a non-excused absence from the final examination.

___*MIDTERM EXAMINATION GRADE:* ___________	25%
___*FINAL EXAMINATION GRADE:* ______________	40%
___*DESIGN PROJECT GRADE:* __________________	25%
___*HOMEWORK GRADE:* _______________________	10%

Prof. John Choma is the Course Lecture Instructor; the Discussion Leader will be announced during the first week of class. Prof. Choma's office hours are difficult to predict accurately and reproducibly but generally, they are from 12:00 -to- 2:00 on Mondays and from 2:00 -to- 5:00 on Wednesdays in Powell Hall of Engineering **(PHE) Room #620**. Appointments for other meeting times can be arranged by telephoning Prof. Choma at **213-740-4692** or by e-mailing him at johnc@usc.edu. The Discussion Leader will also establish regular office hours.

2. Discussion Sections

Weekly discussion sections spearheaded by the Discussion Leader are scheduled for Fridays at 6:00 -to- 6:50 PM in (OHE) Room #136. Additional and optional discussion sections may also be established as the semester progresses. Homework and project assignments are addressed in the discussion sections, as is particularly challenging lecture material. During the first week of the Fall 2011 semester, no Discussion Sections will meet.

3. Study Guidelines and Suggestions

3.1. Spend time reading the *Abstract* of this Course Syllabus, which defines the pedagogy of the course. Conscientious and properly focused students should understand that solutions to engineering analysis and design problems are not the dominant study issue. Particularly important is the ability to develop the insights that enable insightful interpretations of these solutions so that the fruits of analyses foster innovative circuit and system design skills. A matter related to interpretive acuity is the development of capabilities for defining, applying, and assessing meaningful analytical approximations, which are all but mandated if mathematical tractability and engineering understandability are to be assured.

3.2. It is imprudent to view the *10%* weight attached to homework as being sufficiently small to warrant tacit indifference to these assignments. When diligently addressed and considered, the assigned problems provide analytical experience and engineering insights that are likely to prove beneficial for completing the formal examinations. It should also be understood that homework is counted in the compilation of the final course grade only when its average score enhances the final course average. When the homework average degrades an individual final course average, the homework score is not factored into the overall course average, which is then based on an achievable maximum score of *90%,* as opposed to *100%*. In a word, homework scores can only help the student's final grade.

3.3. Engineers rarely work independently. Accordingly, students are encouraged to work in small teams (no larger than four) on homework assignments, assuming, of course, that such collaboration is done intelligently, conscientiously, and in a manner that encourages equal and proactive participation among all group members. Homework teams need only hand in one assignment per group, making sure that the first page of each submitted assignment clearly identifies the names and corresponding student identification numbers of all group participants. Each member of a given group receives the same numerical mark for the given submission. Homework assignments are graded by the Discussion Leader. On the other hand, examinations are graded exclusively by Prof. Choma.

3.4. Do not fall behind in the course lectures and assignments! Advanced electrical engineering classes, such as EE 536a, are hierarchical; that is, the ability to understand material presented in any given week relies strongly on the comprehension of relevant technical matter discussed in preceding lectures or addressed in earlier assignments.

3.5. Try not to miss any scheduled class or any supplementary discussion sections that may be offered! Graduate courses tend to inspire discussions of important tangential material that may not be explicitly addressed in the assigned readings.

3.6. Do not be shy in the classroom about asking questions about material that is not clearly comprehended. If something is not well understood, chances are that many others in class are experiencing similar confusion. Do not be shy about asking for additional assistance and visiting Prof. Choma during regular office hours or at times arranged by appointment.

4. Required Textbook and Suggested References

The required textbook is as follows:

Wai-Kai Chen, *Passive and Active Filters: Theory and Implementations*. New York: John Wiley & Sons, 1986 [ISBN Number 0-471-82352-X]. The assigned chapter readings in the Course Schedule refer to this text. PDF versions of textual course notes are made available to the student online at www.jcatsc.com. These are delineated in the Course Schedule as "Course Notes." Additionally, PDF versions of actual PowerPoint class lectures are made similarly available. These are delineated in the Course Schedule as "Lecture Aids."

The following textbooks contain potentially beneficial reference reading material.

Phillip E. Allen and Douglas R. Holberg, *CMOS Analog Circuit Design*. New York: Oxford University Press, 2003.

Norman Balabanian and Theodore Bickart, *Linear Network Theory: Analysis, Properties, Design And Synthesis*. Beaverton, Oregon: Matrix Publishers, Inc., 1981.

M. J. Buckingham, *Noise in Electronic Devices and Systems*. Chichester, United Kingdom: Ellis Horwood Limited Publishers, 1983.

Mark Burns and Gordon Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*. New York: Oxford University Press, 2001.

W-K Chen, L. O. Chua, J. Choma, Jr., and L. P. Huelsman (editors), *The Circuits And Filters Handbook*. Boca Raton, Florida: CRC/IEEE Press, 1995.

J. Choma, Jr., *Electrical Networks*. New York: Wiley–Interscience, 1985.

J. Choma and W-K. Chen, *Feedback Networks: Theory and Circuit Applications*. Singapore: World Scientific Press, 2007.

K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*. Reading, Massachusetts: Addison-Wesley Pub. Co., 1978.

Dan Clein, *CMOS IC Layout: Concepts, Methodologies, and Tools*. Boston: Butterworth-Heinemann (Newnes), 2000.

R. C. Dorf (editor), *The Electrical Engineering Handbook*. Boca Raton, Florida: CRC Press, 1993.

Arthur B. Glaser and Gerald E. Subak-Sharpe, *Integrated Circuit Engineering*. Reading Massachusetts: Addison-Wesley Pub. Co., 1977.

R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI Design Techniques For Analog And Digital Circuits*. New York: McGraw-Hill Publishing Company, 1990.

A. B. Grebene, *Bipolar and MOS Analog and Integrated Circuit Design*. New York: Wiley–Interscience, 1984.

Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. United Kingdom: Cambridge University Press, 2004.

Gaetano Palumbo and Salvatore Pennisi, *Feedback Amplifiers: Theory and Design*. Boston: Kluwer Academic Publishers, 2003.

Edgar Sánchez-Sinencio and Andreas G. Andreou (editors), *Low–Voltage/Low–Power Integrated Circuits And Systems*. New York: IEEE Press, 1999.

Thomas F. Schubert, Jr. and Ernest M. Kim, *Active And Non–Linear Electronics*. New York: John Wiley & Sons, Inc., 1996.

G. C. Temes and J. W. LaPatra, *Introduction to Circuit Synthesis and Design*. New York: McGraw-Hill Book Company, 1977.

J. Vuolevi and T. Rahkonen, *Distortion in RF Power Amplifiers*. Norwood, Massachusetts: Artech House, Inc., 2003.

The following information is a partial list of relevant journal literature organized loosely among the indicated topical areas.

ACTIVE FILTERS

M. Banu and Y. P. Tsividis, "An Elliptic Continuous-Time CMOS Filter With On-Chip Automatic Tuning," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 932-938, 1984.

A. Baschirotto, G. Cesura, F. Rezzi, and F. Svelto, "Low-Power BiCMOS Continuous-Time Shaping Filter," *IEEE Trans. on Circuits and Systems–II*, vol. 44, pp. 404-406, May 1997.

Y. Chang, J. Choma, Jr., and J. Wills, "An Active CMOS Image Reject Filter," *Journal of Analog Integrated Circuits And Signal Processing*; vol. 28, pp. 41-49, July 2001.

R. L. Geiger and E. Sánchez–Sinencio, "Active Filter Design Using Operational Transconductance Amplifiers: A Tutorial," *IEEE Circuits and Devices Magazine*, pp. 20-32, March 1985.

M. Ismail, S. V. Smith, and R. G. Beale, "A New MOSFET–C Universal Filter Structure for VLSI," *IEEE Trans. On Circuits and Systems*, vol. 23, pp. 183-194, 1988.

CIRCUIT CONCEPTS, THEORIES, MODELS

J. Choma, Jr., "A Generalized Bandwidth Estimation Theory for Feedback Amplifiers," *IEEE Trans. Circuits and Systems,* vol. CAS-31, pp. 861-865, Oct. 1984.

J. Choma, Jr., "Gain and Bandwidth Characteristics of a Variable-Gain, Actively Neutralized, Differential Pair," *IEEE Trans. Circuits and Systems*, vol. CAS-33, pp. 66-71, January 1986.

J. Choma, Jr., "Signal Flow Analysis of Feedback Networks," *IEEE Trans. Circuits and Systems*, vol. 37, pp. 455-463, Apr. 1990.

J. Choma, Jr. and S. A. Witherspoon, "Computationally Efficient Estimation of Frequency Response and Driving Point Impedance in Wideband Analog Amplifiers," *IEEE Trans. Circuits and Systems*, vol. CAS-37, pp. 720-728, June 1990.

P. J. Hurst, "Exact Simulation of Feedback Circuit Parameters," *IEEE Trans. Circuits and Systems*, vol. 38, pp. 1382-1389, Nov. 1991.

P. J. Hurst, "A Comparison of Two Approaches to Feedback Circuit Analysis," *IEEE Trans. Education*, vol. 35, pp. 253-261, Aug. 1992.

P. J. Hurst and S. H. Lewis, "Determination of Stability Using Return Ratios In Balanced Fully Differential Feedback Circuits," *IEEE Trans. On Circuits and Systems*, Part II, vol. 42, pp. 805-817, Dec. 1995.

G. Palumbo and J. Choma, Jr., "An Overview Of Single And Dual Loop Analog Feedback; Part I: Basic Theory," *Journal of Analog Integrated Circuits And Signal Processing*, vol. 17, pp. 175-194, Nov. 1998.

G. Palumbo and J. Choma, Jr., "An Overview Of Single And Dual Loop Analog Feedback; Part II: Design Examples," *Journal of Analog Integrated Circuits And Signal Processing*, vol. 17, pp. 195-219, Nov. 1998.

Y. P. Tsividis, "Integrated Continuous-Time Filter Design—An Overview," *IEEE J. of Solid–State Circuits*, vol. 29, pp. 166-176, Mar. 1994.

J. O. Voorman, "Analog Integrated Filters Or Continuous-Time Filters For LSI and VLSI," *Rev. Phys. Appl.*, no. 22, pp. 3-14, January 1987.

S. A. Witherspoon and J. Choma, Jr., "The Analysis of Balanced Linear Differential Circuits," *IEEE Trans. on Education*, vol. 38, pp. 40-50, February 1995.

CIRCUIT DESIGN METHODS AND EXAMPLES

M. Atarodi and J. Choma, Jr., "A 7.2 GHz Bipolar Operational Transconductance Amplifier For Fully Integrated OTA-C Filters," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 6, pp. 243-253, Nov. 1994.

Y. Chang, J. Choma, Jr., and J. Wills, "A CMOS Monolithic Image-Reject Filter," *Journal of Analog Integrated Circuits And Signal Processing*, vol. 28, pp. 43-51, July 2001.

W. R. Davis and J. E. Solomon, “A High-Performance Monolithic I-F Amplifier Incorporating Electronic Gain Control,” *IEEE J. Solid State Circuits*, vol. SC-3, pp. 408-416, December 1968.

S. R. Jost, “An 850 MHz Current Feedback Operational Amplifier,” *Proc. Bipolar Circuits and Tech. Mtg*., pp. 71-74, 1992.

K. A. Kozma, D. A. Johns, and A. S. Sedra, “Automatic Tuning of Continuous-Time Filters Using An Adaptive Filter Technique,” *IEEE Trans. Circuits and Systems*, vol. 38, pp. 1241-1248, 1991.

L. Luh, J. Choma, Jr., and J. Draper, “A Continuous Time Common Mode Feedback Circuit (CMFB) For High Impedance Current–Mode Applications,” *IEEE Trans. On Circuits and Systems*, Part II, vol. 47, pp. 363-369, April 2000.

C. S. Park and R. Schaumann, “A High Frequency CMOS Linear Transconductance Element,” *IEEE Trans. on Circuits and Systems*, vol. 33, pp. 1132-1138, Nov. 1986.

S. Pipilos, Y. P. Tsividis, J. Fenk, and Y. Papananos, “A Si 1.8 GHz RLC Filter with Tunable Center Frequency and Quality Factor,” *IEEE J. Solid–State Circuits*, vol. 31, pp. 1517-1525, Oct. 1996.

V. I. Prodanov and M. H. Green, “A Differential Active Load and Its Applications in CMOS Analog Circuit Designs,” *IEEE Trans. on Circuits and Systems*, vol. 44, pp. 265-273, Apr. 1997.

J. Silva-Martinez, M. S. J. Steyaert, and W. M. C. Sansen, “A 10.7–MHz 68–dB SNR CMOS Continuous-Time Filter With On-Chip Automatic Tuning,” *IEEE J. of Solid–State Circuits*, vol. 27, pp. 1843-1853, Dec. 1992.

W. M. Snelgrove and A. Shoval, “A Balanced 0.9–μm CMOS Transconductance–C Filter Tunable Over the VHF Range,” *IEEE J. of Solid–State Circuits*, vol. 27, pp. 314-323, Mar. 1992.

S. Szczepanski, J. Jakusz, and R. Schaumann, “A Linear Fully Balanced CMOS OTA For VHF Filtering Applications,” *IEEE Trans. On Circuits And Systems*, Part II: vol. 44, pp. 174-187, March 1997.

Z. Wang and W. Guggenbuhl, “A Voltage-Controllable Linear MOS Transconductor Using Bias Offset Technique,” *IEEE J. of Solid–State Circuits*, vol. 25, pp. 315-317, Feb. 1990.

S. L. Wong, “Novel Drain–Based Transconductance Building Blocks for Continuous–Time Filter Applications,” *Electron. Lett.*, vol. 25, pp. 100-101, Jan. 1989.

A. Wyszyński, R. Schaumann, S. Szczepanski, and P. Van Halen, “Design of a 2.7 GHz Linear OTA and a 250-MHz Elliptic Filter in Bipolar Transistor-Array Technology,” *IEEE Trans. On Circuits And Systems*, Part II: vol. 40, pp. 19-31, Jan. 1993.

5. Course Schedule

In the schedule that follows, reference is made to *Course Notes 1* -through- *9*, as delineated below. These notes are posted in PDF format to the course website, **www.jcatsc.com**, where they can be printed for personal or collegial use. However, be advised that all of these notes are protected by International Copyright Law in that at least portions of each set of notes have either been submitted for publication in archival journals or will appear in textbooks authored by the instructor and published by World Scientific Press (2007) or Cambridge University Press (2011).

COURSE NOTES 1: Linear Two Port Networks: Theory, Models, and Applications.
COURSE NOTES 2: Scattering Parameters: Concept, Theory, and Applications.
COURSE NOTES 3: Passive, Constant Resistance, Broadband Delay Filter.
COURSE NOTES 4: Coupled Inductor, Constant Resistance, Broadband Delay Filter.
COURSE NOTES 5: Passive Filter Characteristics and Interstage Matching Networks for Analog RF Integrated Circuits.
COURSE NOTES 6: Distributed Circuit Models and Applications.
COURSE NOTES 7: Distributed Circuit Architectures for Analog Signal Processing at Ultra High Frequencies.
COURSE NOTES 8: The Modeling of the Monolithic Inductance.
COURSE NOTES 9: Characterization of the Dynamic Range of Active Networks.

In addition, note the Technical Report Section of the website!

WEEK	WEEK OF	LECTURE TOPIC	READINGS
1, 2	08/22/11 08/30/11	TWO PORT NETWORK MODELS & ANALYSIS y–Parameter Model z–Parameter Model Transmission Parameters *Gain Implications* *Impedance Implications* Constant Input Impedance/Admittance Networks	Course Notes 1 Lecture Aid #1 Chapter 1 Chapter 9
3, 4	09/05/11 09/12/11	SCATTERING PARAMETERS One Port Reflection Coefficient Two Port Scattering Matrix *I/O Reflection Coefficients* *Transducer Power Gain* *Feedback Parameter* Relationship To Conventional Two Ports Lossless Two Port Special Case	Course Notes 2 Lecture Aid 2
5, 6, 7	09/19/11 09/26/11 10/03/11	FILTER APPROXIMATIONS Butterworth Maximally Flat Magnitude Chebyshev Filter DELAY FILTERS Active Realization Passive Realization	Chapter 6 Course Notes 3 Course Notes 4 Chapter 7 Lecture Aid #3 Chapter 10
8, 9	10/10/11 10/17/11	DISTRIBUTED NETWORKS Two Port Model Characteristic Impedance Circuit Structures Attenuation Wavelength	Course Notes 6 Course Notes 7 Lecture Aid #4 Lecture Aid #5
	10/13/11 ***10/20/11***	***MIDTERM EXAMINATION*** ***DESIGN PROJECT ASSIGNMENT***	***Open Book***
10, 11, 12	10/24/11 10/31/11 11/07/11	RF MATCHING FILTERS Review Of RLC Circuit Fundamentals Up-Conversion Filter Down-Conversion Filter Broadband Matching *Fundamental Considerations* *Equalizers* *Butterworth & Bessel Broadband*	Course Notes 5 Chapter 9 Course Notes 9 Lecture Aid #6 Chapter 13
WEEK	**WEEK OF**	**LECTURE TOPIC**	**READINGS**
13, 14, 15	11/14/11 11/21/11 11/28/11	TRANSCONDUCTOR-CAPACITANCE FILTERS System Architectures Lowpass Bandpass Notch Circuit Realization	Chapter #16 Lecture Aid #7 Lecture Aid #8 Lecture Aid #9
	12/13/11	***FINAL EXAMINATION (11:00 – 1:00)***	***Open Book***

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01 August 2011

cc. Prof. E-S. Kuh, Department Chair
Dr. Edward Maby, Associate Department Chair
EE 541−Website