EE 477L MOS VLSI Design (elective)

2009 Catalog Data: 477L MOS VLSI Circuit Design (4, FaSp) Analysis and design of digital MOS VLSI circuits including area, delay and power minimization. Laboratory assignments including design, layout, extraction, simulation and automatic synthesis. Prerequisite: EE 328Lx Circuits and Electronics for Computer Engineers or EE 338 Physical Electronics.

Textbook: CMOS Digital Integrated Circuits, 3rd edition, Kang and Leblebici, McGraw-Hill

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Topics:

- Introduction to CMOS Circuits; MOS transistor theory, stick diagrams, transmission gates latches,
- CMOS Processing Technology and Fabrication, CMOS Design Rules
- CMOS Physical Design - Euler Paths, Interconnections, Layout Strategies
- MOS Transistor Theory - IV Characteristics , Capacitance, Threshold Voltage, Scaling, Inverter Characteristics, Transmission Gate Characteristics,
- Inverter Fall Time/Delay, Inverter Optimization, Sequential Circuits, Interconnect Delay, Interconnect Resistance, Capacitance, Superbuffer Design
- Power Consumption
- Dynamic Circuits, Dynamic Storage, Domino logic, Memory Design

Course Objectives: To introduce the topic of VLSI Design, to introduce design constraints and tradeoffs, including economic considerations, to produce engineers capable of designing VLSI cells, to provide design techniques that can be applied as technology evolves, to provide capability for lifelong learning as technology changes

Course Outcomes: The student completing EE 477L should possess the following skills:

(Note by the instructor of the course: these are only the basic skills and after they are completely addressed in our classes, and depending on the number of remaining lectures, the instructor will present a more in depth discussion of some of the topics and/or add some special topics such as static timing analysis, power optimization, etc.)

1 **Digital Logic Design**:
1.1 NAND/NOR Design: The students should be able to convert NAND circuits to NOR circuits and vice versa

2 **Circuit Design:**
2.1 Combinational Circuit Design: The students should be able to do the following:
2.1.1 Provide transistor-level circuits for complementary CMOS NAND, NOR, and transmission gates, inverters, latches, and flip-flops.
2.1.2 Construct full-adder circuits to minimize area or maximize speed
2.1.3 Construct multiplexer circuits with transmission gates

2.1.4 Construct multiplexer circuits with complementary CMOS NAND and NOR gates

2.1.5 Construct compound complementary CMOS gates from Boolean equation specifications and vice versa

2.1.6 Construct a simple XOR gate

2.2 Sequential Circuit Design: The students should be able to do the following:

2.2.1 Construct a circuit for a D flip flop that is positive/negative edge triggered, with asynchronous set/reset and a load signal

2.2.2 Construct asynchronously settable and resettable latches and flip flops

2.3 Circuit Design - Basic understanding of transistors: The students should be able to do the following:

2.3.1 Use unit-size and minimum size transistors in circuits

2.3.2 Identify source and drain of transistors in complementary CMOS circuits and transmission gates

2.3.3 Determine regions of operation of transistors in simple circuits, applying traditional inequalities

2.3.4 Explain the reasons for transmission of weak 1's in NMOS transistors and weak 0's in PMOS transistors

2.3.5 Detect transistors subject to the body effect and know the resultant changes in threshold voltage that occur.

2.3.6 Describe the physical changes that result when a positive voltage is applied to the gate of an enhancement-mode NMOS transistor, including accumulation, depletion and inversion

2.3.7 Locate parasitic MOS and bipolar transistors in simple CMOS layouts

2.3.8 Compute current IDS in MOS transistors based on gate, source and drain voltages

2.3.9 State the relationship between MOS current and voltages, gate capacitance, transistor betas, carrier mobility, device sizes

2.3.10 Apply basic relationships between current flow, voltage and capacitance to analyze circuits

2.3.11 Compute effective channel resistance in the linear region, based on mobility, gate capacitance, channel length and channel width

2.3.12 Take into account channel length modulation when computing current flow in the saturation region

2.3.13 Determine the output voltage of a CMOS pass transistor given an input voltage and gate voltage over time

2.3.14 Determine regions of operation of pass transistors over time, given initial conditions

2.4 Circuit Design – Capacitance and equivalent circuits: The students should be able to do the following:

2.4.1 Compute worst-case gate capacitance using a parallel plate model

2.4.2 Approximate the gate capacitance in the cutoff, linear and saturation regions

2.4.3 Give an equivalent circuit for any MOS circuit, even with long wires

2.4.4 Compute diffusion capacitance given the relevant parameters

2.4.5 State the gross relationship between gate capacitance, diffusion capacitance, channel resistance, interconnect resistance and interconnect capacitance, and the rise/fall/delay for a CMOS circuit

2.5 Circuit Design - The Inverter: The students should be able to do the following:

2.5.1 Identify regions of operation of transistors in an inverter when the inverter is operating in different parts of the input/output transfer curve

2.5.2 Sketch the effect of the beta ratios of inverter transistors on the shape of the input/output transfer curve

2.6 Circuit Design – Delay computations: The students should be able to do the following:

2.6.1 Size transistors in complementary CMOS gates for equal worst case rise/fall times
2.6.2 Identify a critical path in a gate or logic circuit
2.6.3 Use lumped or distributed RC time constants to find critical paths in a logic diagram
2.6.4 Set limits on integration to compute rise/fall/delay for an inverter
2.6.5 Compensate for late and early clocks when designing flipflops
2.6.6 Identify the timing factors that contribute to clock cycle in a flip flop (setup, hold, clock to Q)
2.6.7 Compute lumped and distributed wire delays
2.6.8 Include inductance in an equivalent circuit for a wire
2.6.9 Determine whether L's must be included when modeling a particular situation
2.6.10 Compute Rint and Cint for wires
2.6.11 Estimate fringing field capacitance using a graph or equation
2.6.12 Estimate the RC time constant at any node in an equivalent circuit using Elmore delay even with fan out
2.6.13 Determine when to insert repeaters
2.6.14 Construct an inverter chain to drive a large capacitive load when diffusion capacitance is negligible and when it is not negligible.
2.6.15 Size devices in complementary CMOS circuits using the ratio method
2.7 Circuit design – Power Considerations: The students should be able to do the following:
2.7.1 Identify power consumption situations as static or dynamic
2.7.2 Know the relationship between oxide thickness and leakage power
2.7.3 State the relationship between switching frequency and power

2.8 Circuit design – Noise margins: The students should be able to do the following:
2.8.1 Compute noise margin for a CMOS circuit given VOH, VOL, VIH and VIL
2.8.2 Give definitions for VOH, VOL, VIH and VIL and understand how they can be obtained.

2.9 Circuit design – Dynamic circuits: The students should be able to do the following:
2.9.1 Design and analyze a dynamic latch and flip flop
2.9.2 Identify where charge sharing occurs and compute the effect on the circuit voltages
2.9.3 Construct dynamic and domino logic circuits
2.9.4 Adhere to rules about inputs changing in dynamic and domino logic circuits
2.9.5 Be able to produce timing diagrams for any MOS circuit, including dynamic and domino logic circuits
2.9.6 Construct 6 transistor and 1 transistor RAM circuits, and show timing diagrams for their operation

3 **Physical Design:** The students should be able to do the following:
3.1 Sketch stick diagrams of CMOS circuits using a typical cell design style
3.2 Sketch stick diagrams of compound CMOS gates using Euler paths to organize the physical design
3.3 Define the terms stacked contact, split contact, butting contact, and ohmic contact
3.4 Use a physical layout tool to design CMOS cells
3.5 Design a layout with multiple cells using simple area minimization strategies, including VDD and Gnd sharing, abutting connections, metal layer assignments and cell abutment in one or both directions
3.6 Use the left edge algorithm to connect common inputs/outputs in a routing channel

4 **Fabrication:** The students should be able to do the following:
4.1 Enumerate the steps in fabrication of typical CMOS chips in order
4.2 Enumerate the detailed steps in the photolithographic process
4.3 Understand the reasons for layout design rules
4.4 Show the 3D structure of a CMOS layout along a vertical cut through the substrate
4.5 Define the terms epitaxy, deposition, diffusion, and ion implantation

Laboratory Projects: Three design laboratories, each of which builds on the other, culminating in a project, the objective of which is to minimize the area-delay product. The project itself has a workload roughly equivalent to the 3 lab assignments of the course. The topic of the project will be announced in the second part of the semester, and can be done by groups of two students. More details will be provided later on how the project work should be submitted and presented. The top three designs will receive up to 30% of their project score as extra credit points.

Prepared by: Alice C. Parker **Date**: April 4, 2009
Edited by: Shahin Nazarian **Date: August 25, 2010**