University of Southern California
Viterbi School of Engineering
Ming Hsieh Department of Electrical Engineering

EE 479 - Analog and Non-linear Integrated Circuit Design

Instructor: Ali Zadeh
Email: prof.zadeh@yahoo.com
Lecture Time:
Lecture Classroom:
Term: Fall 2010
Office Hour:
Pre-requisite: EE 348L
Office location:

Pre-requisite:

- Linear-Time Invariant (LTI) systems, Signals and Systems, time domain (t-domain) vs. frequency domain (s-domain) analysis, RLC networks, Laplace transform, KCL, KVL, basic transistor (Diode, BJT, MOS) operations and circuits, basic feedback block diagram.
- If you have no idea about these concepts, do not take the course. If you had these concepts in other courses but you forgot about them, study them as soon as possible.

Required Text Book:

- P. R. Gray, P. J. Hurst, S. H. Lewis, & R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5-th Edition, John Wiley & Sons, Inc., New York, 2009.

Reference Text Books:

- R. Jacob Baker, *CMOS Circuit Design, Layout, and Simulation*, 2nd Edition, IEEE Press, 2005.
- P. E. Allen & D. R. Holberg, *CMOS Analog Circuit Design*, 2nd Ed, Oxford University press, 2002.
- B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw Hill, 2001.
- D. A. Johns & K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, New York, 1997.

Class Website: All the material and announcements will be posted on DEN.
Please check EE 479 Class Website on DEN once a day.

Course Goal:

- EE479 covers analysis and design of Analog and Non-Linear Integrated Circuits. The course consists of two sides of dealing with Analog Integrated circuits: (a) Analyzing a given Analog Integrated circuits through homework exercises and exams. (2) Designing Analog integrated circuit is accomplished by a major final project.

- The emphasis of the course material will be on CMOS analog circuits such as current sources, active load, bias current and voltages, differential pairs, frequency response, feedback amplifiers, output stages, noise behavior, Miller compensation, one-stage and two stage CMOS operational amplifier, folded-cascode, telescopic, operational transconductance amplifier (OTA), high-performance, low-voltage, and high-speed CMOS operational amplifier. We may cover band-gap circuits and voltage references. Finally, we will cover material on the Analog non-linear integrated circuits such as large signal analysis, distortion, and crystal oscillators.

Grade: Final course grade is based on the following formula:

Homework Assignments	=	25%
Midterm I Exam	=	25%
Midterm II Exam	=	25%
Class Project	=	25%
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Total	=	100%

Instructor's Background:

I am a part-time faculty in the Electrical Engineering department. I have worked in Semiconductor industry since 1982 and designed many Analog and Mixed-Signal Integrated circuits: Switched-Capacitor circuits and Filters, Analog-Digital Interface Integrated Circuits, Micro-power Biomedical Data-Converter Integrated Circuits and Systems, and CMOS Image sensors.

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Exams

There will two Midterm exams: The dates of exams are announced in the class schedule. The second Midterm is NOT cumulative. It covers only the material after the first midterm.

Exams will be closed book. Students can bring one 8.5" x 11" page (both sides of the sheet) of notes for the midterms. Paper for exams will be supplied. Just bring a pencil, eraser, and a calculator. You must show how you derived the answers in order to receive full credit.

Homework Assignments

There will be six homework assignments given during the semester. Homework assignments will be given through the class web-site and are due by the announcements. If you cannot make it to the lecture, have a friend to turn in your homework for you.

Homework Policies:

(1) ***Your homework must be professional quality work.***
(2) ***I expect you to spend time on doing your homework assignments.***
(3) Copying homework from each other is considered cheating.
(4) Use only standard 8.5 in x 11 in papers.
(5) Use only one-side of each page.
(6) Put stables on the upper-left corner.
(7) Write nicely, large, neatly and legibly.
(8) Put each LTspice schematics and/or simulation results in separate pages.
(9) Turn in your homework in the classroom at the beginning of the lecture.
(10) Each person turns-in his/her homework individually.
(11) Write your name precisely according to USC records: ***Last Name, First Name.***
(12) Late homework and E-mail homework will NOT be accepted.

LTspice Simulation

- We will be using LTspice for simulations of our circuits, homework and project.
- LTspice can be down-loaded free from Linear Technology, Inc. Website. It has schematic capture, simulations engine, and waveform view. LTspice does NOT have any limitations on the number of transistors in your circuit schematic.
- You have model files for 0.09um (90nm) IBM CMOS technology. This is Level 54 HSPICE (BSIM4V3) parameters, IBM90nm.txt. This model file is from an actual processed wafer lot of IBM provided by MOSIS IC design Services.
- I will provide the model file on the DEN website. Copy the text file "IBM90nm" into your PC and place it in your simulation folder (the folder in which you want your circuit schematics and symbols). Place ".INCLUDE IBM90nm" directive in the schematics.
- You must become familiar to LTspice in terms of: Schematic Capture, Creating SPICE Net-list, simulations, and viewing the waveform. I expect you to learn this as soon as possible. You need to become familiar with simulation tools within two weeks. Some simple circuit schematic will be provided and discussed in the class.
- Use the following website to get all the information about LTspice.

  http://cmosedu.com/cmos1/LTspice/LTspice.htm

- To download the free LTspice software, go to following website:

  http://www.linear.com/designtools/software/

- Six video instruction of how to use LTspice is in this website:

  http://cmosedu.com/videos/LTspice/LTspice_videos.htm

- LTspice User Manual is in this website:

  ltspice.linear.com/software/scad3.pdf

Class Project

One of the main purposes of the course is for student to have hands-on experience in designing a major CMOS Operational Amplifier integrated circuit using LTspice Design Tools.

1. Your project report must be professional quality work.
2. The project report must be done in the MS power-point (.ppt)
3. Handwritten project will NOT be accepted.
4. Either one or two persons can work on the same project. Because of the amount of work, I do recommend two people.
5. A sample report will be provided.

The performance specification of the project operational amplifier is in Table 1. This opamp can be a part of high-speed data-converter circuit used in Imaging Sensor products.

Parameter Description	Required	Achieved	Value	Priority
Power Supply Voltage (Vdd)	1.8	1.8	V	--------
Temperature (Room)	25	25	°C	--------
TSMC 0.18um Process Corner	Typical	Typical	-----	--------
Output Load Capacitor	1	1	pF	--------
Opamp Open Loop DC Gain (Avo)	> 100		dB	**1**
Opamp Unity Gain-Bandwidth Product (UGBW)	> 500		MHz	**1**
Phase Margin	> 60		Degree	**1**
Settling Time (0.01% of 1V input step)	< 5		ns	**1**
Common-Mode Input Range	> 0.75	Vin1-to-Vin2 =?	V	**1**
Supply Current Consumption (Idd)	< 25		mA	**2**
Power Consumption (Vdd X Idd)	< 45		mW	**2**
Positive Slew Rate (SR+)	> 1		V/ns	**2**
Negative Slew Rate (SR-)	> 1		V/ns	**2**
Common Mode Rejection Ratio (at 100Hz)	> 80		dB	**3**
Positive Power Supply Rejection Ratio (at 100Hz)	> 60		dB	**3**
Negative Power Supply Rejection Ratio (at 100Hz)	> 60		dB	**3**

Table 1. CMOS Operational Amplifier Specification for the Class project.

Achieving all these specifications simultaneously will be challenging. Several papers and patents will be provided at the end of the semester to give you some ideas how to push the performance of your circuit. First try to achieve the minimum possible performance. Then, improve the opamp performance if you have additional time.

The class project is graded based on:

Organization and Project Report:	10%
Analysis and Hand Calculations:	10%
Circuit Design Innovation:	10%
Circuits /Test Circuit Diagrams:	10%
Graphs and Waveforms:	10%
Specification Performance:	50%
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Total	**100%**

EE 479 Weekly Schedule, Fall 2010

Week	Tuesday Lecture	Thursday Lecture	Readings
(1)	Introduction: • Syllabus • Analog vs. Digital	Frequency vs. Time Domain: • Linear-Time Invariant (LTI) system • RLC networks	**Chapter 1** LTSpice
(2)	PN Junction., MOS Device: • Ohmic (Triode) Region • Saturation Region	MOS Device: • Small Signal equivalent (Sat. Region). • Transconductace, Output Resistance	**Chapter 2**
(3)	MOS Device 2nd order effects: • Body Effect (γ, χ) • Channel Length Modulation (λ)	MOS Device: • High-frequency model • Gate & Junction Capacitances	**Chapter 3**
(4)	Amplifier Configurations: • Common source (CS) • Common-Gate (CG) • Source Follower (SF)	Multi-Transistor Amplifier: • Cascade Config. • Cascode Config. • Gain enhancement	**Chapter 3**
(5)	Differential Pairs: • Differential Mode • Common Mode	Current Sources: • Cascode • Low-voltage Cascode	**Chapter 4**
(6)	Differential Pair: • Active Load	References: • Current & Voltage	**Chapter 4**
(7)	References: • Self biasing V_T reference • CMOS V_T Reference.	Opamp Specifications: • Single-Ended output • CMRR, PSRR+, PSRR-, CMIR	**Chapter 6**
(8)	Midterm I Review **Midterm I : Chapters: 1, 2, 3, 4**	**Midterm I** **6:00 pm - 7:30 pm**	
(9)	Opamp Topologies: • Telescopic, Folded-Cascode, OTA	Opamp Topologies: • Telescopic, Folded-Cascode,, OTA	**Chapter 6**
(10)	Amplifier Frequency Response: • CS, CG, SF Configurations	Amplifier Frequency Response: • CS, CG, SF Configurations	**Chapter 7**
(11)	Feedback System • Return Ratio • Loop-Gain	Amplifier feedback: • First Order Model. • Gain-Bandwidth Trade-off	**Chapter 8**
(12)	Amplifier feedback: • Second Order Model • Frequency vs. Transient response	Amplifier feedback: • Second Order Model • Frequency vs. Transient response	**Chapter 9**
(13)	Two-Stage Operational Amplifier: • Miller Compensation	Two-Stage Operational Amplifier: • Freq. vs. Trans Response	**Chapter 9**
(14)	Non-Linear Analog Circuits: • MOS Distortion Analysis	Non-Linear Analog Circuits: • MOS Crystal's oscillator.	**Notes**
(15)	Project & Midterm II Review **Midterm II: Chapters: 6, 7, 8, 9**	**Midterm II** **6:00 pm - 7:30 pm**	**Notes**
	Final Project Report due Date:		