EE 454L Syllabus Handout Fall 2010 Instructor: Gandhi Puvvada

Introduction to System Design Using Microprocessors

1. Abstract: This course covers the hardware design of a microprocessor-based system. Students learn interfacing of memory and I/O to 8-bit/16-bit/32-bit processors. Intel processors 8088, 8086, 80386 and 80486 and Intel parallel and serial I/O chips, 8255A and 8251A, interrupt controller 8259A, DMA controller 8237A, bus arbiter 8289 are some of the chips used in this course. Traditional (asynchronous) SRAMs, traditional (asynchronous) DRAMs, Synchronous SRAMs, Synchronous DRAMs, and Flash ROMs are discussed. Interfacing several processors with different data-bus widths to a global memory via a shared bus is also covered.

Students verify their designs through simulation on a CAD tool (ePD). In the lab, students use a microprocessor trainer system together with an 80-channel logic analyzer to build and test circuits interfacing I/O chips to the microprocessor's system bus.

This course is a must for anyone who wishes to acquire an in-depth knowledge of standard chips in a microprocessor-based system, their function, and how to interface them to a microprocessor.

This knowledge is also useful to students interested in SoC (System on a Chip) design. Most of the functions such as UART (serial communication function), which were available in the form of separate chips before (8251A for example), are now available as IP cores (intellectual property cores). A SoC designer will take these cores and interface to the processor core to build the SoC, which is essentially the same as what is taught in this course.

2. Course administration

a) Course prerequisites: EE201L Introduction to Digital Circuits and EE357 Basic Organization of Computer
Systems are the *necessary* prerequisites.
Undergraduate students without these prerequisites will not be able to do this course. This is a hardware course. CS/BME students with no prior hardware design experience, no prior experience with oscilloscopes/logic analyzers, or no prior experience in analyzing and interpreting timing waveforms will need to work hard to come to the level of the other EE/CECS students. Students are expected to have attained hardware design skills through EE201L and EE357.

b) Lecture and labs: http://www.usc.edu/academics/classes/term_20103/classes/ee.html

Lec	**30509R**	**02:00-03:20pm**	**MW**	**VHE217**
Lab	**30602R**	**05:00-08:00pm**	**W**	**VHE205**
Lab	**30562R**	**05:00-08:00pm**	**Th**	**VHE205**

http://www.usc.edu/academics/classes/term_20103/calendar.html

Nov 12	Last day to drop a class with a mark of "W"

c) Examinations: No make up exams.

Final Exam schedule: http://www.usc.edu/academics/classes/term_20103/finals.html

Exam	Date	Day	Time	Note
Midterm	11/1/2010	Monday	1:00-3:20PM/2:00-4:20PM	Extended hours
Final	12/10/2010	Friday	02:00-4:30 PM	Extended hours

d) Grading Policy:

Tentative Weights of course components:
Midterm Exam **~25%** No make-up.
Homeworks **~10%** (penalty for late submission: up to 10% per day if solution has not been distributed)
Lab Experiments **30% to 35%**** (penalty for late submission: 3% per day up to a max. of 7 days. Your TA may refuse to accept labs late by more than 7 days. Even if he/she accepts such very late labs, he/she will apply 5% per day penalty for the 8th day onwards.)
Lab TA's discretionary points **5%** ***
Final exam **~30%** No make-up exam.

** We will be using ePD (electronic Product Designer) together with Synopsys SmartModel library of behavioral models for processors, memories, and peripheral chips to do a number of design exercises.
Hardware building labs deal with interfacing I/O chips to the system bus of an 8086 microprocessor.

*** Your Lab TA will assign points out of the 5% TA's discretionary points based on his/her observation of how well you have understood the labs and how well you performed in the lab. Your TA will be asking you to explain your work to make sure that you did NOT copy your lab work. Please do not get offended.

e) Academic Accommodations:

Any student requiring academic accommodations based on a disability is required to register with Center for Academic Support and Disability Services and Programs (CAS & DSP) each semester. A letter of verification for approved accommodations can be obtained from (CAS & DSP).
Please be sure the letter is delivered to me as early in the semester as possible (no less than 2 weeks before an exam).
The CAS & DSP office is located in STU 301 and is open 8:30 a.m. - 5:00 p.m., Monday through Friday.
Their phone number is (213) 740-0776.
http://sait.usc.edu/academicsupport/centerprograms/dsp/home_index.html

f) Miscellaneous administrative matters:

Lecture class attendance, penalty for absence, and minimum required performance:
http://www-classes.usc.edu/engr/ee-s/454/EE454L_attendance.html

If you miss more than 2 lecture meetings, you will start noticing that you are falling behind.
If you miss more than 5 lecture meetings, you may as well drop the course.
It is a design course requiring continuity in your learning process. So please attend every lecture meeting.

Penalty for lecture absence: 1% for 5th, 6th, 7th, 8th, 2% for 9th and after.
We take attendance in the lab sessions also. You need to make up any missed lab sessions.

Minimum requirements to pass the course:

One needs to get at least **60%** on homeworks, **70%** in lab, a passing grade (D) on the midterm and final examinations,
70% attendance in the lecture class, and **90%** attendance in the lab session to pass the course.

Academic Integrity:

You may be allowed to use the Intel Manuals (listed later), a TTL manual, data sheets for chips such as 8251A, etc.,
on the tests. Classnotes, lab manual, Textbook, homeworks, lab reports, etc. are ***not*** allowed on the exam.
Homeworks are considered to be individual effort. However you are encouraged to share your thoughts with
others. Hardware labs performed in the lab (VHE205) and simulation exercises (on ePD or ModelSim) are considered to be
teamwork. Lab reports: The TA will specify for each lab if the reports have to be completely individual or one combined-report per team or partly individual and party combined. Absolutely no copying.

Academic dishonesty cases will be dealt with severely. You may have gone through the short presentation on
Academic Integrity at USC at Academic Integrity Tutorial and Quiz - Fall 2010 posted on your DEN Blackboard if you are part of a DEN course.
A tutorial is also posted at http://usccollege.na4.acrobat.com/academicintegrity. Another important
resource is the Student Judicial Affairs and Community Standards (SJACS) Website, http://www.usc.edu/student-affairs/SJACS/index.html . You may also want to visit http://www.usc.edu/student-affairs/SJACS/pages/students/community_standards.html
University policy requires that all academic integrity violations must be reported to Student Judicial Affairs and Community Standards (SJACS).

We will try to make the assignments due on times far from the class time.
This is to make sure that students do not miss classes/labs to complete the assignments.

Please check your email regularly. Also visit the blackboard (https://blackboard.usc.edu/) regularly.

g) Instructor: Gandhi Puvvada (email: gandhi@usc.edu)
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Office hours: **10-12 Wed, Thurs**.;
http://www-classes.usc.edu/engr/ee-s/457/Gandhi_Office_Hours.pdf
Home phone number: (310) 839-3933 (up to 10:00PM any day including weekends/holidays)

Students are encouraged to discuss any difficulties they are facing in this course with any of us (TA(s) or grader or myself).

h) Teaching Assistants:

1. "EE454L Lab TA -- Mehrdad Najibikohnehshahri" najibiko@usc.edu
Office Hours:
Please make appointments with the TA through email for additional help.

i) Grader:

EE454L HW Grader -- Manish Harnur harnur@usc.edu
Office Hours: TBA

3. Laboratory schedule:

Your attendance is noted by your TAs. You are not expected to miss any of the lab sessions. If you miss more than two lab sessions, or if you do not complete more than two lab experiments/simulation experiments, you may be disqualified from the course.

Lab Manuals: Please buy the following from the university bookstore.
Lab Experiments (required); Datasheets (required)
Intel Manuals: Your TA may be issuing some Intel manuals.
Return all items at the end of the semester.

Labs:

Lab order Lab #

A. 0. Introduction to EE454L lab.
Setup student accounts for ePD (electronic Product Designer)

B. 1. Introduction to Logic Analyzer and EPROM access time measurement

C. ** 3. Introduction to the ESA86/88-3

D. 21. Parts 0, 1, 2, and 3
Introduction to using Synopsys SmartModel library components (processor, memory, etc.) in board-level simulation in ePD

E. 21. Parts 4 and 5
Wait-state generator

F. ** 26. Design of a Memory/IO controller to interface slow SRAMs and slow I/O chips to Intel 80486

G. 5. Conditional and Unconditional I/O

H. ** 30. Flash Memory interface

I. 21A. Simulation exercise on 8255A (parallel interface)

J. ** 27. Bursting and Address pipelining using Synchronous SRAMs

K. 23. Simulation exercise on 8259A (interrupt controller)

L. ** 23a. Cascading of the Programmable Interrupt Controller - 8259A

M. 25. Simulation exercise on 8251A (serial interface)

N. ** 25a. Serial Communication with 8251A using ESA 86/88

O. ** 28. Bus Arbitration exercise

P. ** 24. DMA Controller

Problems with ePD? Please go to http://www-classes.usc.edu/engr/ee-s/457/ePD_problems.html

4. Readings:

Please read your classnotes (lecture notes) regularly. Reading on a regular basis is very important for this course. Students lagging behind in the course will very soon fall out of step and will not be able to catch up.

Primary References:
Class Notes and Lab Manual (required): Please buy from the university (USC) bookstore.
Secondary Reference:
Textbook (optional): The 80x86 Family Design, Programming, and Interfacing (Second Edition) By John Uffenbeck**.**

5. Course Schedule/Topics:

# of Lec. Topic

1 Lec. 1. Course introduction, Review of basic TTL components and board-level design issues

1 Lec. 2. SRAM, EPROM, building larger memories from smaller memory chips

2 Lec. 3. Memory interfacing to 8-bit/16-bit/32-bit byte addressable processors, Exhaustive and partial address Decoding

1 Lec. 4. 8088/8086 microprocessor, bus cycle, pin definitions, Memory Space, I/O Space, system bus signals, Demultiplexing of multiplexed address/data lines

1 Lec. 5. Clock generator, Ready and Reset synchronization, Wait state generator

1 Lec. 6. Buffering and bidirectional buffer for data lines

2 Lec. 7. I/O PORTs, memory mapped vs. isolated I/O, unconditional and conditional I/O, status register, port construction examples, 8-bit I/O interfacing to 16-bit and 32-bit processors

1 Lec. 8. Timing specs of a microprocessor and timing specs of a memory. Board-level timing design/check.

2 Lec. 9. Programmable Parallel Interface, 8255A

0.5 Lec. 10. Min and Max mode of 8088, 8288 bus controller

0.5 Lec. 11. Burst bus cycles of 80486

1.0 Lec. 12. Pipelined bus cycles of 80386

0.5 Lec. 13. Synchronous SRAMs

0.5 Lec. 14. Flash ROMs

1.5 Lec. 15. Traditional DRAMs, /RAS, /CAS, FPM (Fast Page Mode), Refreshing

0.5 Lec. 16. Synchronous DRAMs

3 Lec. 17. Vectored interrupts, Interrupt Controller 8259A

1 Lec. 18. Serial Interface, 8251A, Timer/Counter 8254A

3 Lec. 19. DMA, Direct Memory Access controller 8237A

1 Lec. 20. Byte swapping, 32/16/8-bit bus conversion

2 Lec. 21. Multibus, 8289A Bus Arbiter

1 Lec. 22. Microcontrollers (if time permits)